12-2001

Design and analysis of an attenuator-based, four-channel, differential, 150 MHz, linear-in-dB VGA with sub-nanosecond delay dispersion for PET applications

Bryan Scott Puckett
University of Tennessee

To the Graduate Council:

I am submitting herewith a dissertation written by Bryan Scott Puckett entitled "Design and analysis of an attenuator-based, four-channel, differential, 150 MHz, linear-in-dB VGA with sub-nanosecond delay dispersion for PET applications." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

James Rochelle, Major Professor

We have read this dissertation and recommend its acceptance:

Accepted for the Council:

Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

To the Graduate Council:

I am submitting herewith a dissertation written by Bryan Scott Puckett entitled "Design and Analysis of an Attenuator-Based, Four-Channel, Differential, 150 MHz, Linear-in-dB VGA with Sub-Nanosecond Delay Dispersion for PET Applications." I have examined the final paper copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Dr. James Rochelle, Major Professor

We have read this dissertation
and recommend its acceptance:

Accepted for the Council:

Vice Provost and
Dean of Graduate Studies

Design and Analysis of an Attenuator-Based, Four-Channel, Differential, 150 MHz, Linear-in-dB VGA with Sub-Nanosecond Delay Dispersion for PET Applications

A Dissertation
Presented for the
Doctor of Philosophy
Degree
The University of Tennessee, Knoxville

Bryan Scott Puckett
December, 2001

Acknowledgments

I would like to thank my Major Professor, Dr. James Rochelle for his guidance in this project and for all of the instruction he provided both inside and outside of the class room during my graduate studies. I would like to thank the members of my committee, Dr. Alexiades, Dr. Islam, and Dr. Newport for their suggestions and work reviewing this document. I would like to thank Dr. David Binkley for his guidance and mentoring at Concorde Microsystems. I would also like to thank my friends at Concorde. Robert Nutt for making the financial side of things possible and less worrisome. Brian Swann for his encouragement, technical advice, and many discussions. Paul Ullrich for his help with the test boards and schematics. Dr. Stefan Seigel for his help understanding the basics of PET. And Dr. Ben Blalock for his encouragement and help.

I would also like to remember Dr. T.V. Blalock who was originally on my doctoral committee. He was a great mentor, professor, counselor, and friend, who greatly influenced my education beginning at the undergraduate level and continuing throughout my graduate work.

Finally, I would like to thank my wife Nicole for her help and patience during the many late nights and months without weekends.

Abstract

Positron Emission Tomography (PET) is a medical imaging methodology based on the measurement of the concentrations of a positron-emitting radioisotope inside a three dimensional object. PET systems require hundreds of channels of high performance detector readout electronics. The Phase I ASIC was developed in 1992 to reduce the cost, power consumption and complexity of PET systems and to improve reliability. The Phase I ASIC has been very successful and is a key component in thousands of commercial PET units currently in use.

A Phase II ASIC is now under development because the architecture of the Phase I ASIC is not compatible with the higher count rates made possible by a new detector material LSO and the digital integration requirements of a new generation of LSO-based PET medical imaging systems. Additionally, new data processing techniques and new silicon processes can now be employed to produce a lower cost design with improved performance.

The objective of this research is the development and analysis of a four-channel VGA system that meets the new architectural and performance specifications of the Phase II ASIC. The design, analysis, and simulation of an attenuator-based VGA system is discussed and the experimental results from two prototype chips is presented.

Table of Contents

List of Tables

List of Figures

Chapter 1 Background

1.1 Overview of PET

Positron Emission Tomography (PET) is a medical imaging methodology based on the measurement of the concentrations of a positron-emitting radioisotope inside a three dimensional object. The concentrations are measured by detection of coincident 511 keV gamma rays (photons) emitted during beta decay of the radioactive tracer. During the nuclear decay, a proton decays to a neutron by emitting a positron and a neutrino. The positron or beta particle travels a small distance and annihilates with an electron producing two coincident 511keV photons. Conservation of momentum requires the coincident gamma rays produced during the beta decay of the tracer to be emitted in opposite directions (180 degrees apart) in the center of mass frame of the electron/positron pair. A ring of detectors collects these coincident photons, and an "event" is defined as the detection of a gamma ray of appropriate energy by two opposing detectors during a small time interval known as a coincidence window and is illustrated in Fig. 1.1. The event is considered to have occurred at some point along the line defined by the two detectors. By storing thousands of events a sinogram is produced, which can be used to reconstruct a three dimensional image of the tracer concentrations. [1, 2]

1.2 PET Detector Components

Detectors for PET are usually composed of scintillating crystals (often more than one) coupled to one or more Photomultiplier Tubes (PMTs) [3]. The scintillating crystals

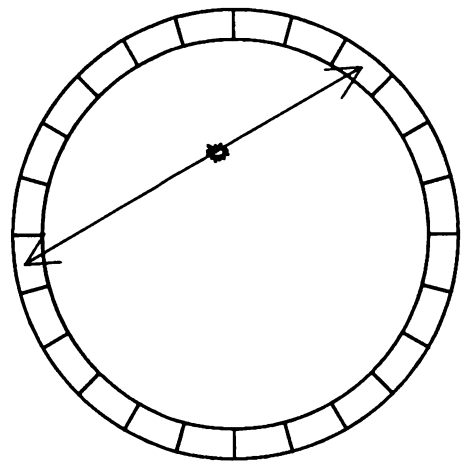


Fig.1.1 Ring of Detectors Capturing a Coincidence Event.

absorb the 511keV photons produced by the beta decay and emit photons of visible light [4]. This light passes through the faceplate of the PMT as shown in Fig. 1.2. and strikes the photocathode, which emits electrons via the photoelectric effect [5]. These electrons are focused and accelerated toward the first dynode. During this acceleration, the electrons gain enough kinetic energy to liberate multiple electrons when they strike the surface of the first dynode; thus an electron multiplication effect is produced. The electrical potentials of the dynodes are arranged so that the electrons emitted from one dynode are accelerated toward the next dynode. During each transition from dynode to dynode the electrons gain enough energy to continue the multiplication process. At the end of this cascade multiplication process, the anode collects a large current pulse that is proportional to the number of photons emitted by the scintillator and thus proportional to the energy of the detected gamma ray.

The present generation of PET scanners uses detectors based on crystalline Bismuth

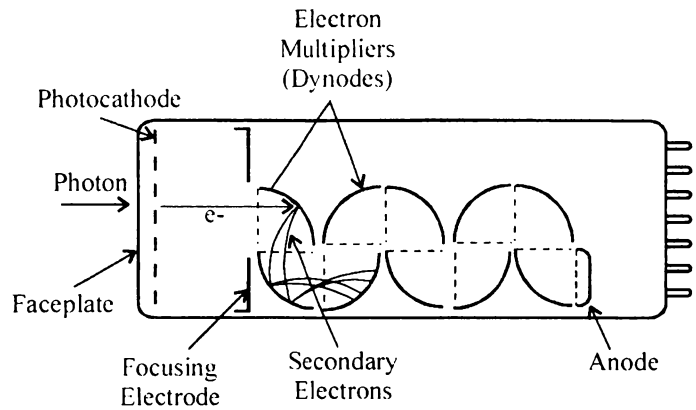


Fig.1.2 Photomultiplier Tube (PMT).

Germanate (BGO). BGO is an inorganic scintillating material that produces photons with wavelengths of 400 – 600 nm when struck by gamma rays. BGO has good stopping power for 511keV gamma rays due to its high density and the high atomic number of Bismuth (83). Thus, a 511keV gamma ray that enters the BGO crystal has a high probability of being absorbed before passing out the other side. BGO has a moderate light yield which is approximately 20 – 25% of the light yield of NaI scintillators. The signals produced by a BGO based detector have decay times of approximately 300 ns at room temperature. [6].

The next generation of PET scanners will use detectors based on Lutetium Oxyortho-silicate (LSO). LSO is a scintillating material with decay times of approximately 40 ns, stopping power similar to BGO, and significantly higher light output compared to BGO. Fig. 1.3 shows a simulation comparing normalized amplitude pulses for LSO and BGO based detectors. The faster decay time of the LSO based detectors allows better count rate performance, but also necessitates faster pulse processing electronics. The higher peak

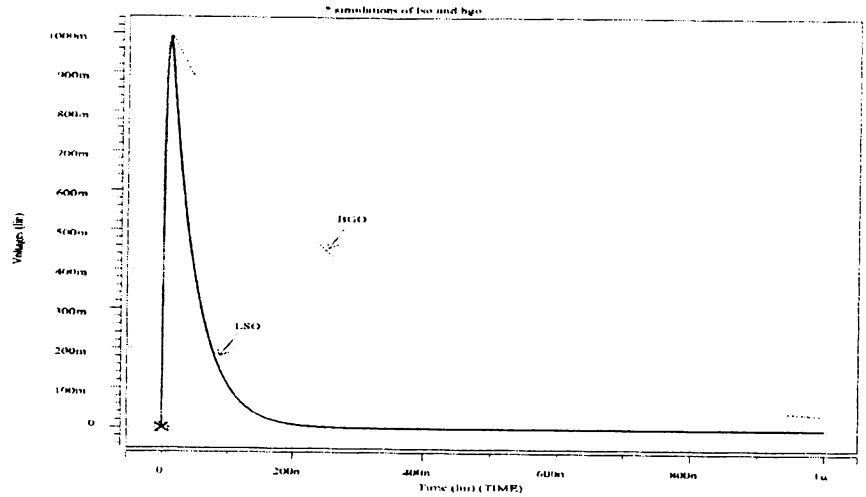


Fig.1.3 Comparison of Normalized LSO and BGO Output Pulses.

light output of the LSO produces a larger signal to noise ratio, which allows better timing resolution and thus narrower time coincidence windows.

1.3 Block Detector Concept

Four PMTs are often coupled together as a block detector to increase the spatial resolution of the PET system [7]. A typical block detector is shown in Fig. 1.4 and consists of a scintillating crystal array and four PMTs. A single scintillating crystal is typically cut part way through to form an array of 8 x 8 pixels connected at the base. The crystal array is optically coupled to four PMTs, which are in turn connected to the analog processing electronics. The signals from all four channels are processed using Anger logic [8] to determine the time, location and energy of the detected photon. The total number of photons produced by the scintillating material is proportional to the energy of the detected gamma ray. The photons are divided between the four PMTs by the scintillator array and

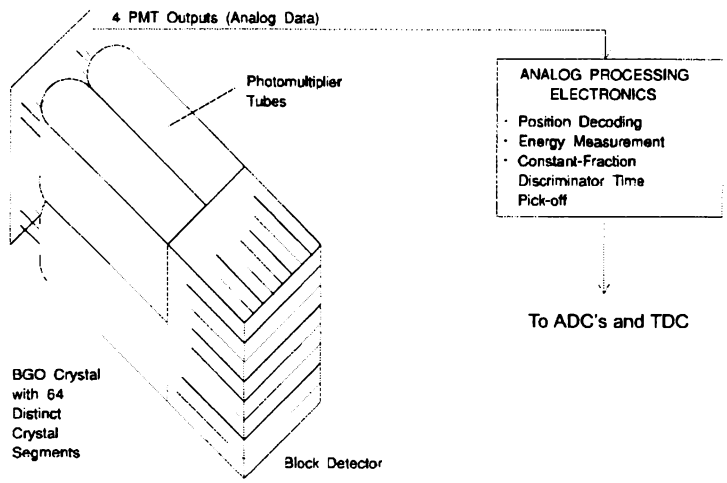


Fig.1.4 Block Detector and Associated Analog Signal Processing Requirements [7].

each of the PMTs produce an output current pulse whose total charge is proportional to the number of photons collected by that tube. Thus, the sum of all four of the PMT output pulses can be integrated to produce a voltage that is proportional to the energy of the initial gamma ray. Position decoding is accomplished by comparing the ratio of the number of photons collected by two adjacent PMTs to the total number of photons collected by all four PMTs. Consider the block detector shown in Fig. 1.5, the x position of the detected gamma ray can be found by examining the ratio

$$R_X = \frac{A+B}{A+B+C+D},$$

and the y position can be found from the ratio

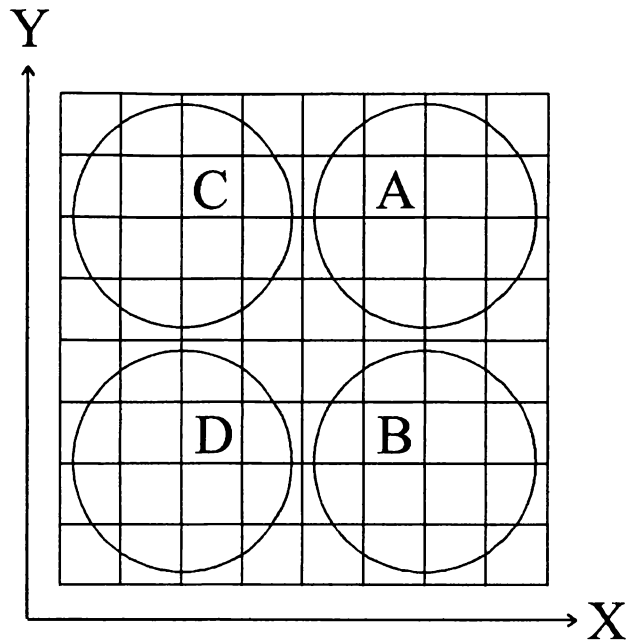


Fig.1.5 Rear View of Block Detector [10].

$$R_Y = \frac{A+C}{A+B+C+D}.$$

A one dimensional probability distribution function is shown in Fig. 1.6. The peaks represent the probability that the gamma ray was detected in a particular row (or column) of the array as a function of the ratio R_X (or R_Y). The timing information is produced by summing the outputs of all four PMTs and using this signal as the input to a Constant Fraction Discriminator (CFD). The CFD generates a time mark that is relatively independent of signal amplitude [9]. The spatial resolution is improved in a block detector because the light from a single pixel in the scintillator array is divided between the four PMTs and comparison of the four signals allows determination of which pixel was struck by the

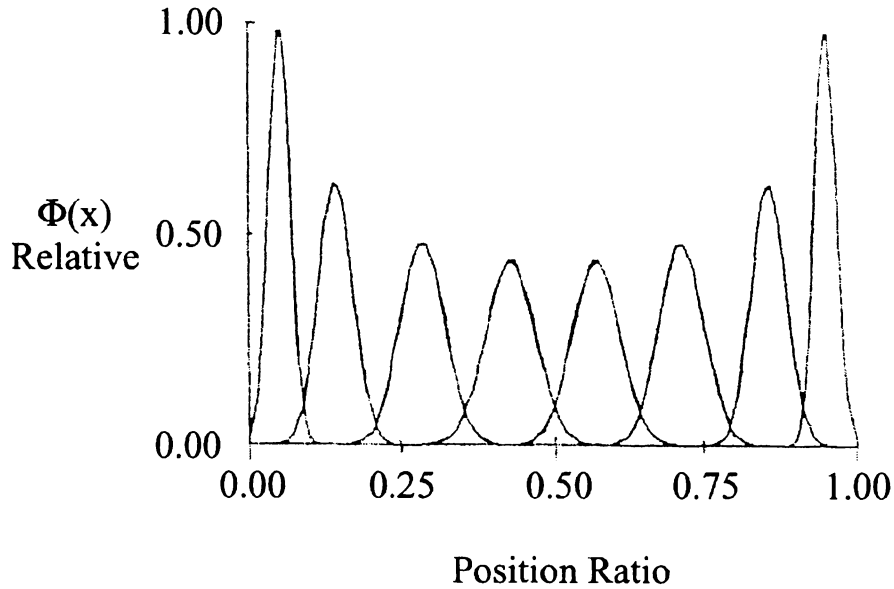


Fig.1.6 Probability Distribution Function for an 8-Crystal Row (or Column)[10].

gamma ray. Thus, the 64 pixels of the array can be resolved instead of only four pixels represented by the PMTs.

1.4 Phase I Block Detector Front-End ASIC

All of the high performance electronics shown in Fig. 1.7 is required for each of the hundreds of block detectors in a typical PET scanner. In the first PET systems, these circuits were composed of discrete components. The discrete designs were complex and expensive to fabricate and also required large amounts of power and board area. The number of components for a single block detector channel was approximately 250 which impaired reliability since component interconnect is often the largest contributor to system failure. An Application Specific Integrated Circuit (ASIC) based design could cut the

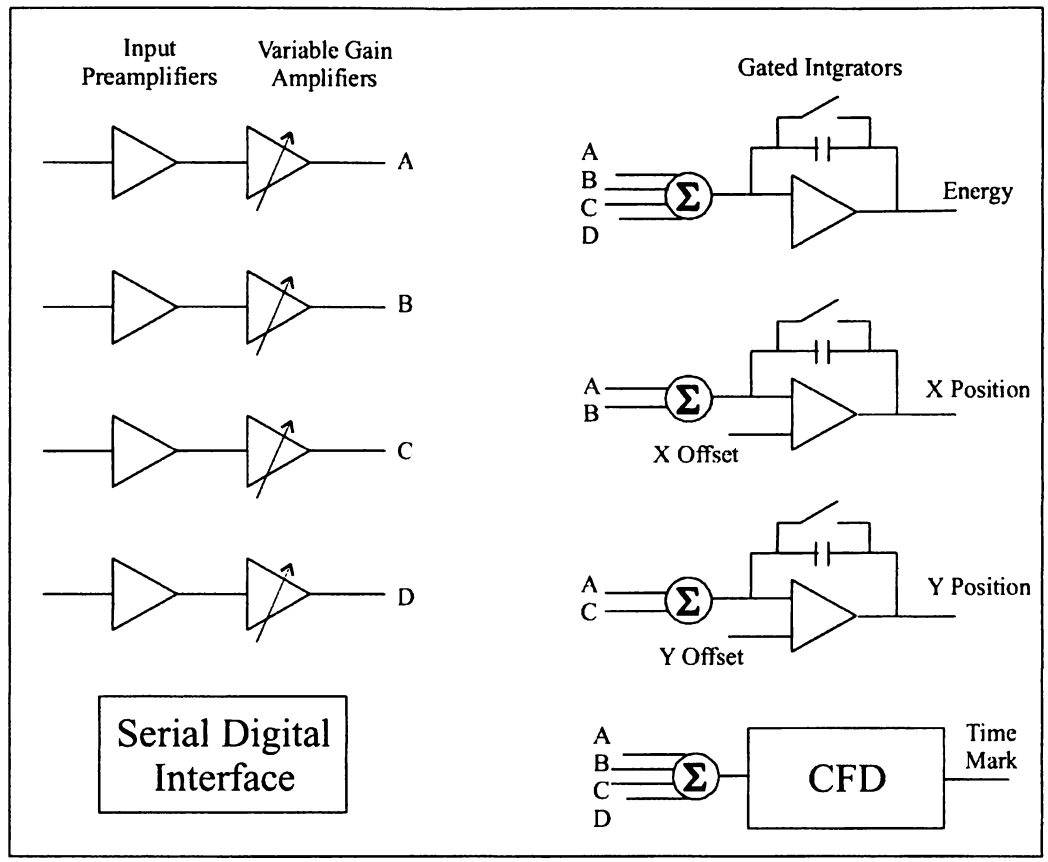


Fig.1.7 Phase I Front-End ASIC Block Diagram.

component count to approximately 50-75, which would improve reliability and greatly reduce area, cost, and power consumption [11].

In 1992 CTI Inc. developed an ASIC based design for the block detector front-end electronics for the purpose of reducing the cost, size and power consumption of the PET systems [7]. The Phase I chip includes four single-ended, current-input preamplifiers, four Variable Gain Amplifiers (VGAs), signal summers, integrators, a CFD, and a serial digital interface as shown in Fig. 1.7. The signals from the PMTs are connected to the inputs of the preamplifiers that add additional gain to improve the signal to noise ratio of the channel. The outputs of the preamplifiers are connected to the VGAs, which are needed to equalize the gains between the four channels because the PMT gains are typically not well matched from tube to tube. The serial digital interface allows the VGA gains to be programmed with a minimal number of I/O pins. The ASIC processes the four current signals from the PMTs and produces a digital time mark and three analog outputs representing the energy, x-position, and y-position of the detected gamma ray. All four channels are summed to produce the input to the CFD, which produces the digital time mark. Each of the three analog outputs are voltages derived by integrating the charge in a current pulse. The x-position output is proportional to the current pulse produced by summing the A and B channels, the y-position output is proportional to the current pulse produced by summing the A and C channels, and the energy output is proportional to the current pulse produced by summing all four channels. An off-chip Time to Amplitude Converter (TAC) and an Analog to Digital Converter (ADC) process the digital time mark and generate a binary number representing the time at which the gamma ray was detected. Off-chip

ADCs are also used to digitize the energy, x-position, and y-position analog output signals.

The Phase I ASIC has been very successful and is a key component in thousands of commercial PET units currently in use. However, the chip is nearly 10 years old and has remained virtually the same since its initial development. New data processing techniques and new silicon processes can now be employed to produce a lower cost design with improved performance. Also the architecture of the Phase I ASIC is not compatible with the high count rate and digital integration requirements of a new generation of LSO-based PET medical imaging systems.

1.5 The Proposed PET Phase II ASIC

A new Phase II front-end ASIC is under development using a 0.5 micron, mixed-signal CMOS process to meet the architectural and count rate performance requirements of the next generation of LSO-based PET scanners. The major architectural changes include: the single-ended current inputs are replaced by differential voltage inputs, the energy and timing signal summers and integrators are moved from on-chip analog processing to Digital Signal Processing (DSP) in the host computer, the Time to Digital Converter (TDC) is on-chip, and the dual 5v supplies are replaced by a single +5v supply.

As with many other signal processing applications, advances in DSP has facilitated the migration of many of the analog signal processing functions previously performed in the Phase I chip from on-chip analog processing to DSP functions performed in the system processor. For example, the analog integration performed by the Phase I ASIC has been replaced by digital integration in the host computer interfaced to the Phase II ASIC. This

migration provides more flexibility since the specific processing functions are defined by re-configurable software rather than by custom hardware.

Another motivation for a new chip is the availability of newer silicon processes. The Phase I chip is fabricated in a 2 micron CMOS process. By moving to a process with 0.5 micron feature sizes the bandwidth of the analog circuits can be increased, the propagation delay of the digital gates can be reduced, and the required die area can be reduced. The smaller die area reduces cost and also improves yield.

Finally, the adoption of LSO based detectors for the new systems allows for much higher count rates but requires a corresponding improvement in the count rate capacity of the pulse processing electronics. The Phase II ASIC was designed before LSO was available and thus was never intended to process data at the count rates made possible by LSO. A higher count rate allows more samples to be taken in the same amount of time. Thus, images can be acquired in less time, which improves patient throughput and cost efficiency. Alternatively, the higher count rate allows imaging with lower tracer doses for pediatric and small animal imaging in which reduced radiation exposure of the patient is more critical.

A block diagram of the architecture planned for the Phase II front-end AISC is shown in Fig. 1.8. The chip includes four differential, voltage-input VGA's, four energy channel anti-aliasing filters, a timing channel signal summer, a CFD, a TDC, and various test, bias and control circuits. The VGA's each have a differential voltage input and two differential current outputs, one for timing and one for energy. The timing outputs of all four VGAs are summed to produce a timing channel input signal for the CFD. The output of the CFD supplies a digital time mark for the TDC, and the TDC produces a binary number repre-

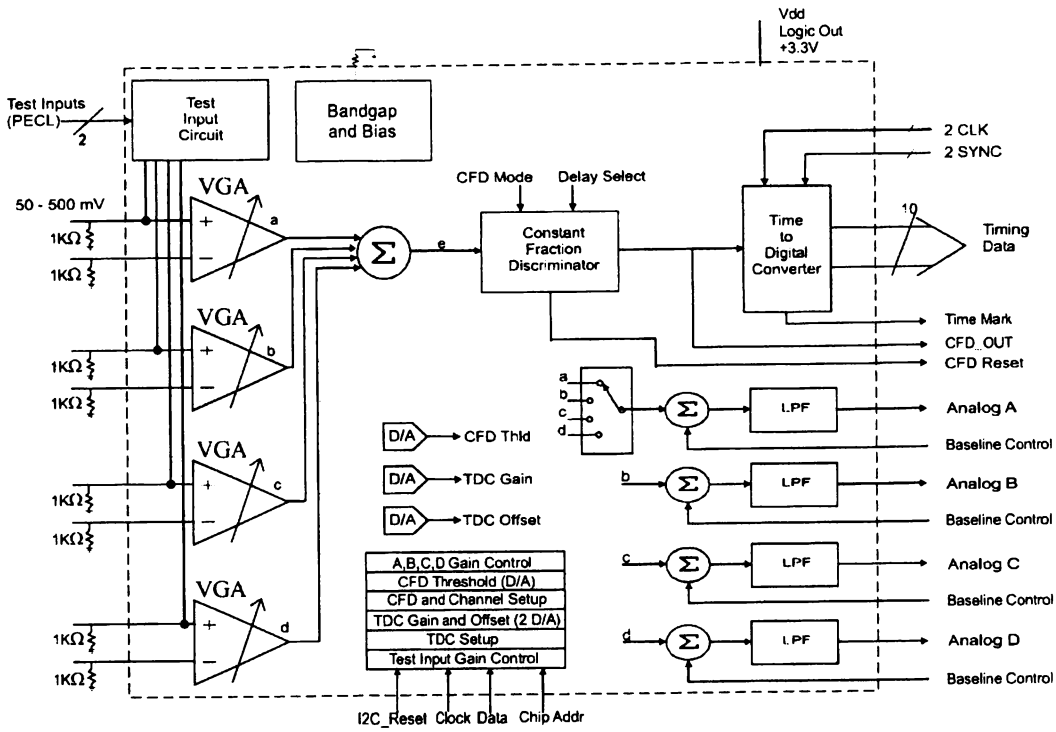


Fig.1.8 Proposed Phase II Front-End ASIC Block Diagram.

senting the time when the event was detected. The energy channel outputs of the VGAs are low-pass filtered to prevent aliasing and are converted to voltages that are digitized by off-chip ADCs.

1.6 Phase II VGA requirements

The VGA's for the Proposed Phase II chip have the following requirements:

- Gain Range of 1x to 10x programmable in 10% Steps,
- (linear in dB with ~ 0.83dB steps),

- Low Signal Propagation Delay Dispersion Over the Gain Range (<1ns),
- Differential Voltage Input with CM Range Including Ground,
- Common Mode Rejection Ratio (CMRR) of –10dB at 100MHz,
- Input Resistance Compatible with 75ohm Termination,
- Differential Current Output,
- 100MHz + Bandwidth,
- Relatively Low Noise (10nV/rt-Hz),
- Single +5V Supply.

The selectable gain must cover a coarse range of 1:10 with each gain setting increasing the gain by a factor of 1.1 over the previous gain setting. This implies a gain that is linear in dB with 25 steps of approximately 0.83dB. Because a host computer sets the gains automatically, the gain settings must be monotonic so that the gain selection algorithms do not fail. The delay dispersion over the entire gain range must be less than 1ns so that changing the gain will have minimal effect on the channel-to-channel time alignment of the system.

The input signals are pseudo differential voltage signals in which one side of the signal is a ground referenced, single-ended signal and the other side is ground. This pseudo differential signal is transmitted from the off-chip PMT preamplifiers to the VGA on twisted pair cables. Any common mode (CM) noise picked up by the cable must be rejected by the

differential inputs of the VGA. To provide appropriate high frequency CM noise rejection, the common mode rejection ratio (CMRR) of the system must be at least –10dB at 100MHz. The CM level of the pseudo differential input signal requires that the CM input range of the VGA include ground. The input resistance of the VGAs must be predictable enough to allow reliable termination of the 75ohm twisted pair cables that carry the PMT signals to the VGAs. The cable termination resistance is set by placing an off-chip resistor in parallel with the input resistance of the VGAs. If the chip-to-chip variation of the input resistance of the VGAs is high, the input resistance of the VGAs must be large so that the resistance of the parallel combination is dominated by the off-chip resistor and the variation of the termination resistance is reduced.

Current outputs are required for each VGA channel because 100MHz current signals can be summed by simply connecting the outputs together, while 100MHz voltage signals require the use of a summing amplifier. A 100MHz system bandwidth is necessary for the timing channel to preserve the fast rising edges produced by the detectors. This requires the VGA bandwidth to be greater than 100MHz because the other circuitry in each channel will reduce the timing channel bandwidth to less than that of the VGAs alone. The fast rise times combined with an equivalent input noise of less than 10nV/rt-Hz are necessary to keep the timing uncertainty (jitter) at an acceptable level.

There are several reasons why the Phase I chip's variable gain design cannot be rescaled for use in the Phase II chip. The Phase I chip has a single-ended current input instead of the differential voltage input required for the Phase II chip. Also, the Phase I chip operates on ± 5v supplies and the Phase II chip operates on a single + 5v supply. Single supply operation limits the available voltage headroom and further complicates a re-

design effort. Another problem is that random offsets in the Phase I topology can produce unpredictable gains from chip to chip especially at low gain settings where a large offset can produce a gain whose polarity is opposite that of the desired gain. All of these factors combined warrant the investigation of a new topology better suited to the Phase II requirements.

1.7 Research Objective

The objective of this research is the development and analysis of a four-channel VGA system that meets the new architectural and performance specifications of the Phase II ASIC discussed above. The VGA system is shown in Fig. 1.9 and is the circuitry to the left of the heavy dashed line.

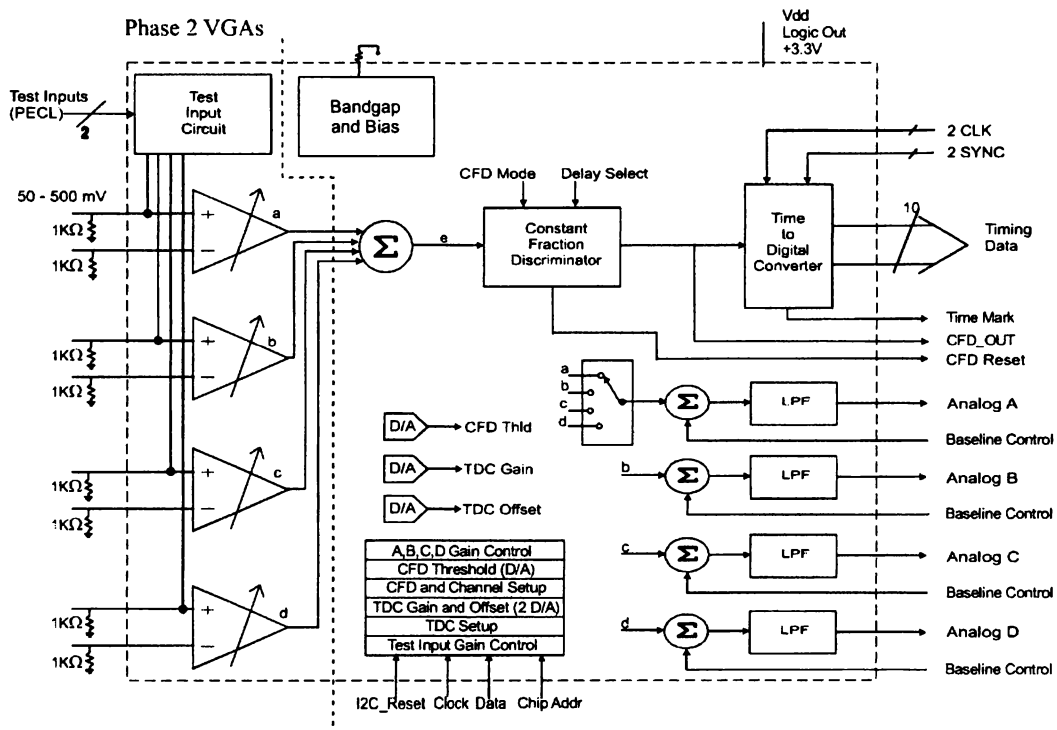


Fig.1.9 Phase II Front-End ASIC Block Diagram Showing VGA Portion of the Circuit.

Chapter 2 Literature Review

2.1 Introduction

The first step in developing a new VGA for the Phase II front-end ASIC is a survey of the relevant VGA literature. There are many different topologies used to realize VGAs. Common approaches use analog multipliers, variable transconductors, variable loads, variable feedback, and attenuator networks. As discussed earlier, the requirement of a summed output that combines the energy signals from all four channels implies a current output for the VGAs. Thus since the inputs are specified to be differential voltages, the selected VGA architecture must include a voltage to current conversion.

2.2 Analog Multiplier Based VGAs

Analog multiplier based VGAs are typically a variation of the Gilbert gain cell [12-23]. As shown in Fig. 2.1, the Gilbert cell is composed of three differential pairs. For the bipolar gain cell shown:

$$\Delta I_{out} = (I_{C3} + I_{C5}) - (I_{C4} + I_{C6}) = (I_{C3} - I_{C6}) + (I_{C4} - I_{C5}) = I_{EE}[\tanh(\frac{V_1}{2V_T})][\tanh(\frac{V_2}{2V_T})]$$

For small signal operation, this can be approximated by

$$\Delta I_{out} \approx I_{EE}(\frac{V_1}{2V_T})(\frac{V_2}{2V_T})$$

This approximation will not hold for the signal levels and 1:10 gain range required for the Phase II VGA. Thus, to be a candidate architecture for the Phase II chip the circuit must be linearized.

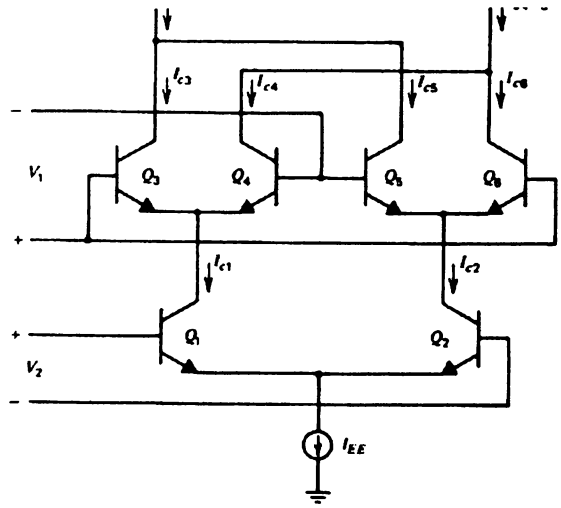


Fig.2.1 Gilbert Cell Multiplier [12].

Various methods have been employed to linearize the Gilbert Cell and typically use another circuit to produce a signal proportional to the inverse hyperbolic tangent of the original signal [12]. This allows linear operation for a much larger signal and gain control range making the circuit useful for VGA applications.

Similar topologies can be used to produce a CMOS, linearized, four-quadrant multiplier that could be used in the VGA for the Phase II chip [24].

Multiplier-based VGAs can be high bandwidth circuits, but are often very complex. They usually have differential current outputs that are compatible with the Phase II design requirements, but the gains are typically process and temperature dependent. Offsets can be a major problem, especially for low gains since the offsets can produce a gain of opposite polarity from the one desired. For example, suppose V_2 is used as the gain control voltage. If the differential pair composed of transistors Q_1 and Q_2 has an offset voltage of V_{off2}, then the effective gain control voltage is $V_2 + V_{off2}$. To select a small positive gain V_2 is set to a small positive value. If V_{off2} is negative and has a magnitude larger than V_2,

the effective gain control voltage is negative and the gain is of opposite polarity compared to the desired gain.

2.3 Programmable Transconductor Based VGAs

Programmable transconductor based VGA's typically adjust the transconductance of the input stage by changing the bias current in the input devices, or programming a degeneration element in the input stage [25-30]. An example of varying the transconductance by adjusting the bias current is shown in Fig. 2.2. The transconductance of the differential pair M2A and M2B is adjusted by varying the bias current I2Ic1. The square law behavior of MOS transistors causes the transconductance of the differential pair to be proportional to the square root of the bias current. Problems with this approach include limited gain

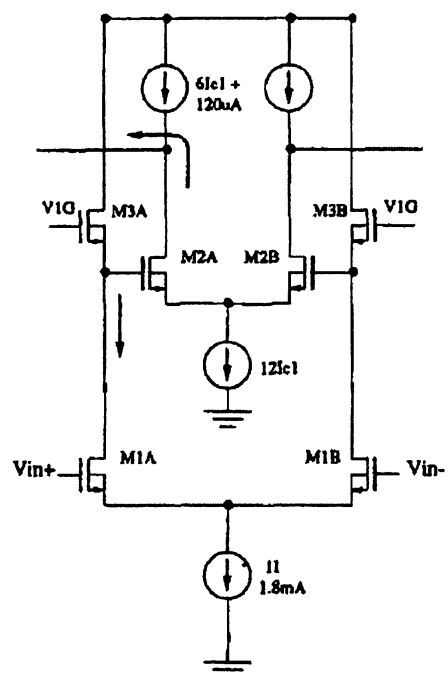


Fig.2.2 VGA Cell Using Variable Transconductance and Variable Loads [26].

range often requiring multiple stages, and limited linear regions. The limited gain range is a result of the square-root dependence of the transconductance on bias current. To increase the gain by a factor of 2x the current must increase by a factor of 4X, thus large gain ranges require too much variation in bias current. For the 10:1 gain range needed for the Phase II VGA, this approach would require multiple stages and would be difficult to make monotonic. An example of adjusting the transconductance using variable degeneration is shown in Fig. 2.3. This approach improves the linearity of the transconductor, but still does not provide sufficient gain range. Other approaches to varying the transconductance include the use of multiple input devices as shown in Fig. 2.4 [31-33] and changing the resistive element in a resistor based transconductor as shown in Fig. 2.5 [24]. These approaches have much better linearity, but typically have lower bandwidths and degraded noise performance due to the larger number of input devices that contribute parasitic

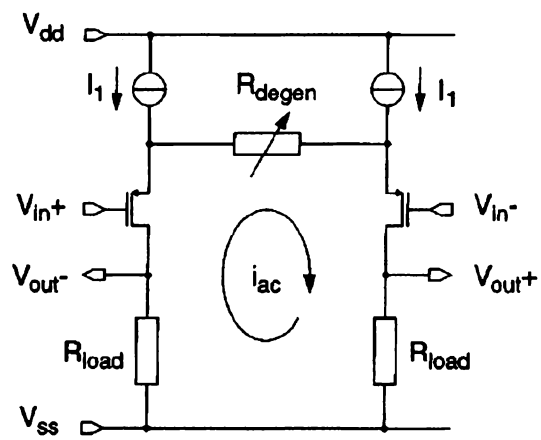


Fig.2.3 Changing Transconductance by Varying the Degeneration [28].

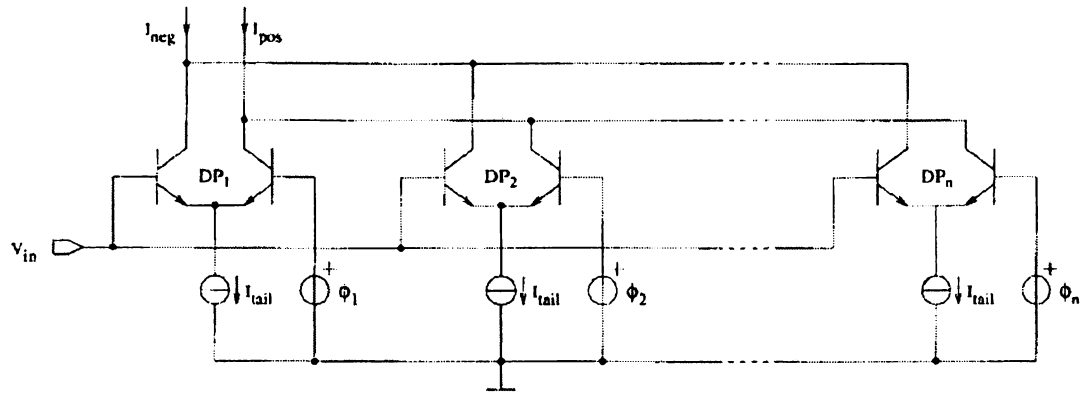


Fig.2.4 Varying Transconductance Using Multiple Input Devices [32].

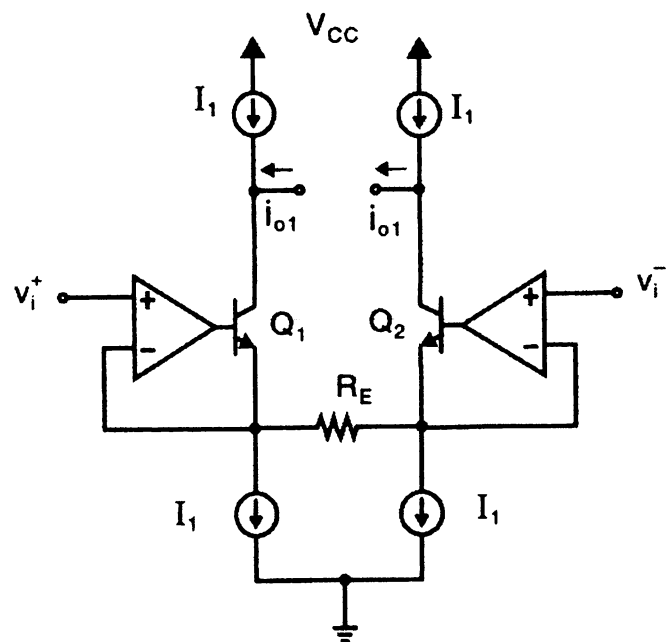


Fig.2.5 Resistor Based Transconductor [24].

capacitance and noise. These architectures all provide the current outputs required by the Phase II VGA design, but would be difficult to implement with sufficient gain range, linearity, bandwidth, and noise performance.

2.4 Programmable Load Based VGAs

Programmable loads [25-26,34] can be used to vary the gain of an amplifier stage. The adjustable loads can be ohmic mosfets as shown in Fig. 2.2 or switched resistive networks. The circuit in Fig. 2.2 uses both variable transconductance and variable loads to provide variable gain. The variable loads are the transistors M3A and M3B, which are operating in the ohmic region. Changing the gate voltage V1G of the transistors varies the resistance of the loads. An undesirable feature of this type of VGA is excessive delay dispersion variation over the gain range due to changes in bandwidth associated with the change in loading. The bandwidth is set by the resistor-capacitor (RC) time constant of the load. The capacitance at the output is essentially unaffected by the gain setting, but the load resistance is clearly directly proportional to the gain. Thus the gain-bandwidth product of the VGA is essentially constant and the bandwidth is inversely proportional to the gain. For the low delay dispersion required by the Phase II VGA, an almost constant bandwidth is essential, and thus a variable load based architecture is not suitable.

2.5 Programmable Feedback Based VGAs

Programmable feedback [35-37] can be used to implement variable gain. The feedback elements can be ohmic mosfets or a switched resistive network. For a voltage feedback amplifier with a constant gain bandwidth product, the result is a bandwidth that

decreases as gain increases, resulting in poor delay dispersion characteristics. Changing the compensation of the amplifier along with the gain setting could possibly reduce this effect by increasing the gain bandwidth product as the gain increases. The VGA reported in [37] is shown in Fig. 2.6 and is based on an operational amplifier shown in Fig. 2.7 that uses switches to reduce the compensation capacitance for higher gains. This variable compensation maintains the bandwidth of the VGA between 17.5 MHz and 35 MHz over a 3:1 gain range. This approach is not practical for the Phase II VGA, which has a bandwidth greater than 100MHz, because the parasitic capacitance of the switches would degrade the bandwidth performance. Additionally, the circuit in [37] has a bandwidth that varies by a factor of 2 over a 3:1 gain range. A 2x bandwidth variation is more variation than is acceptable over the entire 10:1 gain range of the Phase II VGA, and thus this variable compensation approach is not suitable for the Phase II VGAs. For single ended amplifiers, a current feedback configuration can be used resulting in a constant bandwidth over the gain range. However, current feedback amplifiers are typically higher noise circuits than their voltage feedback counterparts and are not readily compatible with a differential design.[38] Additionally, a feedback amplifier based VGA would also need a transconductance stage to perform the voltage to current conversion required for this design.

2.6 Programmable Attenuator with Gain Stage VGAs

Attenuators combined with gain stages can be used to implement programmable gain [38-43]. In this approach, a tapped network of resistors is used to provide the various attenuation levels. The attenuation is set by resistor ratios and is thus very predictable over temperature and process variations. The resistor network is typically either a series ladder

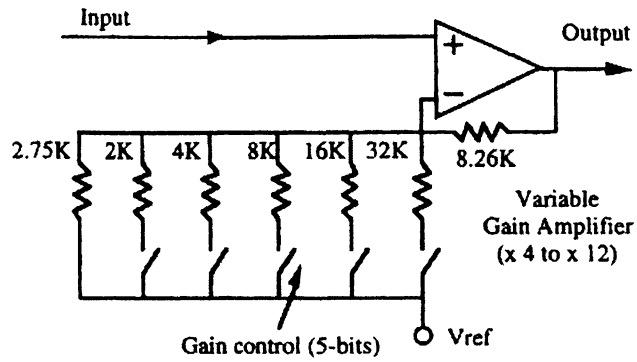


Fig.2.6 Variable Feedback Based VGA [37].

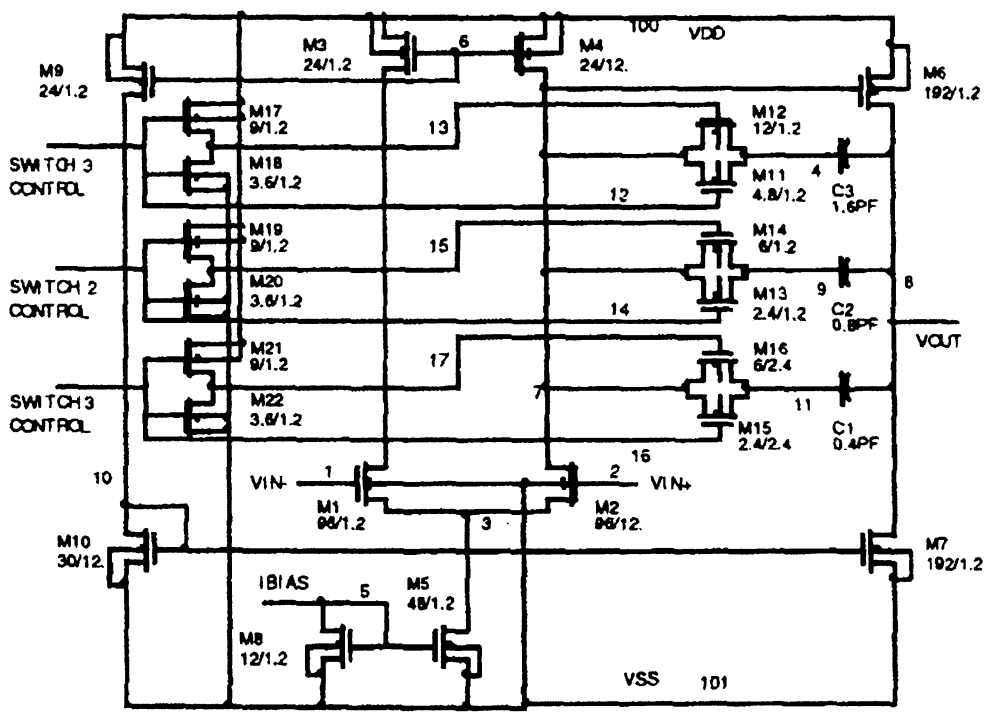


Fig.2.7 VGA Operational Amplifier with Selectable Compensation

as shown in Fig. 2.8 or an R-2R ladder as shown in Fig. 2.9. The series ladder maybe composed of resistors having the same resistance value, resulting in taps with linearly spaced attenuation steps, or the resistor values can be chosen to produce non-linear attenuation steps. The input resistance of the series ladder is equal to the sum of the resistances of the component resistors. The R-2R ladder and its variants inherently have logarithmic attenuation steps. Each stage of the R-2R ladder contributes an attenuation factor of ½ resulting in an attenuation for the N^{th} tap of $(½)^N$. The input resistance of the R-2R ladder is 2R. In [40] a differential R-2R ladder is described that is used in the AD604 VGA. The paper reports a bandwidth of 60-70 MHz for the AD604 that is nearly constant over the 40 dB-gain range. The circuit is based on an earlier "X-AMP" architecture used in the AD600/602/603. The original X-AMP architecture appears to have been based on a VGA reported in [41] which uses an interpolated ladder attenuator and reported a bandwidth of 20 MHz. In [42] a fully differential R-2R ladder based VGA is reported with a bandwidth of 160 MHz and an attenuation range from 0 to 36 dB in 6 dB steps. These results suggest it should be possible to design a differential attenuator followed by a transconductor out-

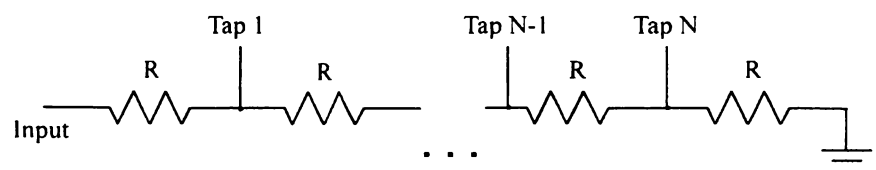


Fig.2.8 Series Ladder Linear Attenuator.

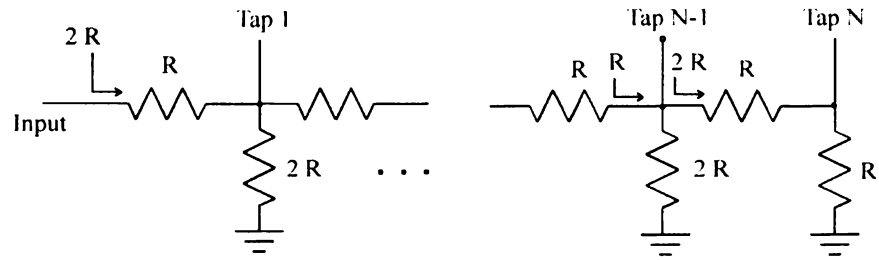


Fig.2.9 R-2R Ladder Attenuator.

put stage that can meet all of the requirements for the Phase II VGA. Such an attenuator based VGA has several desirable features including gain defined by resistor ratios, inherently monotonic gain values, nearly constant bandwidth, and a wide linear input range with a minimal linear input range required for the transconductor stage.

2.7 Literature Review Summary and Proposed Phase II VGA Architecture

Of the various VGA architectures considered above, only the analog multiplier based and the attenuator VGA architectures appear to be useful for the Phase II VGA application. The programmable transconductance based architectures have insufficient gain range, linearity, bandwidth, and noise performance. The variable load based architectures have bandwidths that are inversely proportional to the gain settings and thus cannot provide the low delay dispersion required by the Phase II VGA. The variable voltage feedback based architectures have too much bandwidth variation over the gain range and the current feedback architectures are not well suited for differential applications and have poor noise characteristics. Multiplier-based VGAs can supply the required bandwidth, low delay dispersion, current outputs and noise performance required by the Phase II VGA as

was shown by the Phase I VGAs. The primary problems with the multiplier based VGAs are complexity, gains that are typically process and temperature dependent, and the effect of offsets. Offsets can be a major problem, especially for low gains since the offsets can produce a gain of opposite polarity from the one desired. These undesirable qualities of the multiplier based VGAs justify the investigation of a new VGA architecture. Of the reported attenuator based VGAs discussed above, none are exactly what is needed for the Phase II VGAs. Some of the designs are single-ended, some have only 20MHz bandwidth, one is differential and has the required bandwidth and gain range but does not have the fine ~1dB gain steps required by the Phase II VGA. However, most of the desired characteristics for the Phase II VGA are present in at least one of the reported attenuators. This suggests that with careful design, it should be possible for an attenuator followed by a transconductance stage to meet all of the Phase II VGA requirements.

Based on the literature survey, the best VGA architecture for the Phase II ASIC would appear to be a VGA composed of a programmable attenuator followed by a differential transconductor. This approach appears to be the best because of the simplicity of the design, the inherent monotonicity of the attenuator, and the well-defined gain over process variations.

Chapter 3 Design, Analysis, and Simulation

3.1 Overview of the Architecture

The selected architecture for the Phase II VGA consists of passive, polysilicon, resistive attenuators followed by a fixed-gain, tuned, differential-pair transconductor as shown in Fig. 3.1. The design of each of these components is considered below.

3.2 Attenuator

3.2.1 Attenuator Design Issues and Selection

Resistor Technology Overview

Typically, on-chip passive attenuators are composed of polycrystalline silicon (polysilicon) resistors. A simple polysilicon resistor structure is shown in Fig. 3.2. Polysilicon is usually highly doped to increase its conductivity and is isolated from the substrate by an oxide layer. The resistance of a rectangular object can be described by,

$$R = \rho\frac{L}{A} = \rho\frac{L}{WT},$$

where ρ is the resistivity of the material, L is the length, W is the width and T is the thickness of the object. For a constant thickness this can be reduced to

$$R = \frac{\rho L}{TW} = K\frac{L}{W},$$

where K is the sheet resistance in Ω/square. The resistance characteristics of polysilicon layers are typically reported in this manner. The polysilicon resistors are separated from the conducting substrate by a thin insulating oxide forming a parallel plate capacitor with the oxide acting as the dielectric. The capacitive characteristics of the polysilicon layers

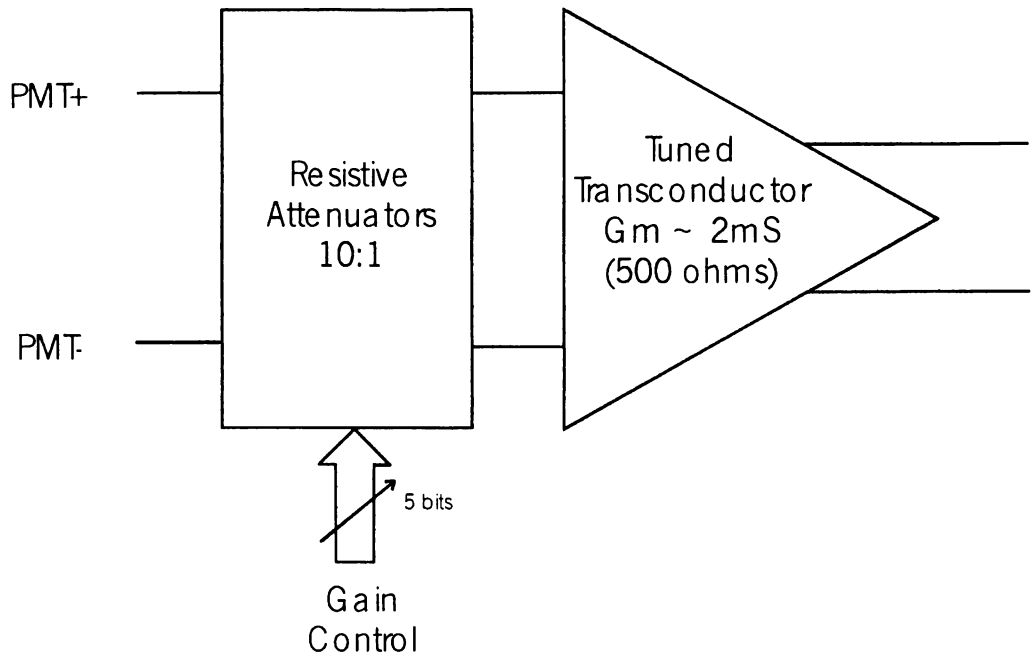


Fig.3.1 VGA Block Diagram.

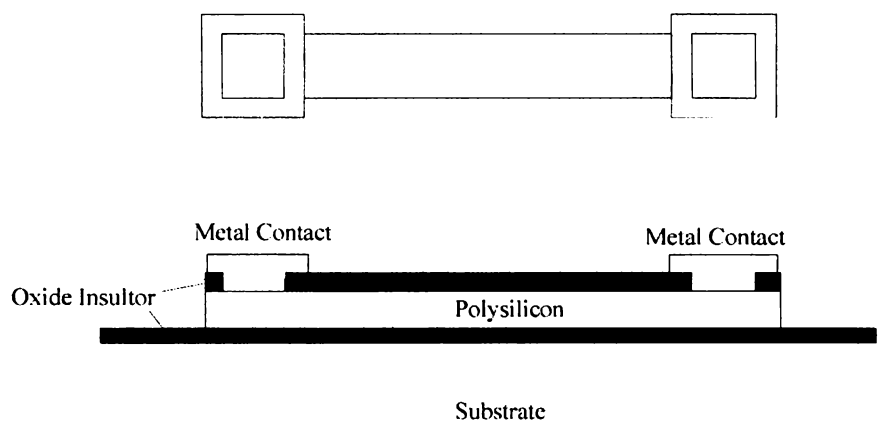


Fig.3.2 Typical Polysilicon Resistor Layout (Top View and Cross Section).

are typically reported as two separate parameters, an area capacitance in farads/μm^2 and a fringe capacitance in farads/μm. The absolute value of polysilicon resistors can vary as much as ± 20% from chip to chip due to processing variations. However, with careful lay-out resistor matching on a single chip can be as good as 0.2% [44].

In order to achieve good matching the resistors in a layout should each be composed of an integer number of unit resistors that are all exact replicas of each other. For example, a 1.5 KΩ resistor and a 3.5KΩ resistor can be fabricated from a 500Ω unit resistor using 3 and 7 unit resistors respectively. Another way to improve resistor matching is to make the resistors physically as large as possible, which helps reduce the effect of small, localized differences in the unit cells. However, the improvement in matching provided by larger dimensions comes at the expense of silicon area and reduced bandwidth due to the larger parasitic capacitance resulting from the larger area. Another issue in polysilicon resistor matching is the resistance of the metal-to-polysilicon contacts used to connect the resistors to the rest of the circuit. The variation and mismatch in the resistance of the metal-to-polysilicon contacts in a unit cell is often significantly higher than the variation and mismatch in the resistance of the polysilicon portion of the unit cells, thus the relative contribution of the contact resistance to the total unit cell resistance should be minimized to improve the unit cell matching.

Because of the relatively large capacitive coupling between the polysilicon layer and the substrate, polysilicon resistors must be modeled as distributed R-C delay lines when the AC characteristics of the resistors are of interest. For this project, each unit resistor is modeled as five segments, each of which is represented by the HSPICE wire model [45]. The HSPICE wire model is based on the Pi network shown in Fig. 3.3. The resistor and

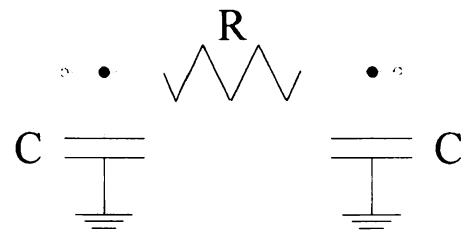


Fig.3.3 HSPICE Pi-Network Wire Model.

capacitors are calculated from the length and width of the given resistor segment and from the sheet resistance, area capacitance, and edge capacitance data from the foundry specifications for the process.

The 0.5μ mixed-signal CMOS process chosen for the Phase II ASIC provides two primary layers, poly1 and HR-poly, that can be used to produce polysilicon resistors. Poly1 is used to fabricate the transistor gates and is a standard layer that is typically available in any CMOS process. MOSIS test results for the poly1 layer in the chosen process report a sheet resistance of approximately 25 Ω/square and a parasitic area capacitance of approximately 87 aF/μm^2. The poly1 layer is doped to reduce its sheet resistance. HR-poly is a specialized polysilicon layer that is masked during the doping process. Because HR-poly is not doped, its sheet resistance remains high. HR-poly layers are typically only available in analog and mixed-signal CMOS processes, and often the sheet resistance of this layer varies widely from process to process. MOSIS test results for the HR-poly layer in the chosen process report a sheet resistance of 1200Ω/square and a parasitic area capacitance of approximately 87 aF/μm^2. The limited availability of the HR-poly layer makes moving

a design using HR-poly to a new process more difficult than moving a design using only standard CMOS layers. Thus, for best portability of the design from process to process, HR-poly should be avoided.

Primary Attenuator Performance Issues

The most important attenuator attributes are the gain step accuracy, bandwidth, delay dispersion, noise, and input resistance. The desired attenuator gain settings are given in Table 3.1. The exact gain steps are not critical and thus can be approximated to within a small gain error if necessary. However, the gains as a function of gain code must be monotonic to allow gain selection to be performed by a host computer. The bandwidth of the attenuator should be much larger than the bandwidth of the transconductor so that the VGA bandwidth is dominated by the bandwidth of the transconductor and remains nearly constant over the gain range. Minimizing the bandwidth variation of the VGA over the gain range helps to reduce the delay dispersion. The delay dispersion of the VGA is required to be less than 1ns over the full gain range. The low delay dispersion is necessary so that the gain can be adjusted without requiring the PET system coincidence timing to be recalibrated. The noise power at the output of the attenuator is roughly the thermal noise associated with the thevenin equivalent resistance for the selected tap plus the thermal noise associated with the on-resistance of the gain select switch. For low noise, the thevenin resistance and thus the total resistance of the attenuator should be minimized. However, the input resistance of the attenuator must be large compared to the desired input termination resistance so that variation of the input resistance has minimal effect on the cable termination. An input resistance of 1 kΩ was chosen as a reasonable compromise

Table 3.1: Desired Attenuator Gain Steps

Tap Number	Attenuation Factor
0	1.000
1	0.909
2	0.826
3	0.751
4	0.683
5	0.621
6	0.564
7	0.513
8	0.467
9	0.424
10	0.386
11	0.350
12	0.319
13	0.290
14	0.263
15	0.239
16	0.218
17	0.198
18	0.180
19	0.164
20	0.149
21	0.135
22	0.123
23	0.112
24	0.102
25	0.092

between resistor noise and termination error. Several topologies were considered for the resistive attenuator. These topologies include an R-110R ladder, a tapped series ladder composed of parallel and series combinations of a unit polysilicon resistor, and a continuous, tapped polysilicon resistor. The R-110R ladder attenuator naturally has gain settings that are linear-in-dB and can be implemented as a practical circuit with no gain approximations. The two series attenuators require some gain approximations as described below to produce a real-world circuit.

Table 3.2 shows the necessary resistor values for a series attenuator with the desired gain steps and an input resistance of 1kΩ. However, in a practical circuit the fabricated resistors should each be composed of an integer number of some unit resistor so that matching is optimized, and the unit resistor should be at least one square and preferably more to reduce the effect of the contact resistance on the resistor to resistor matching and on the absolute magnitude of the input resistance. The combination of these two constraints makes the ideal realization impractical. Two approaches with approximated gain steps were investigated. The first approach was to approximate the desired resistors with a series/parallel combination of unit resistors. The other approach was to use an integer number of unit resistors with no contacts on the ends to approximate the desired resistors.

3.2.2 Preliminary Analysis of the R-110R Attenuator

The R-110R ladder shown in Fig. 3.4 has gain steps that are by nature linear in dB and theoretically can provide the exact gain steps desired with no approximations. The Phase II attenuator requires 25 taps not including the input tap. The input resistance was chosen to be 1 kΩ by considering the trade-off between a predictable input termination and atten-

Table 3.2: Series Resistor Values for Linear in dB Steps

R25	90.90909
R24	82.64463
R23	75.13148
R22	68.30135
R21	62.09213
R20	56.44739
R19	51.31581
R18	46.65074
R17	42.40976
R16	38.55433
R15	35.04939
R14	31.86308
R13	28.96644
R12	26.33313
R11	23.9392
R10	21.76291
R9	19.78447
R8	17.98588
R7	16.3508
R6	14.86436
R5	13.51306
R4	12.2846
R3	11.16782
R2	10.15256
R1	9.2296
R0	92.296

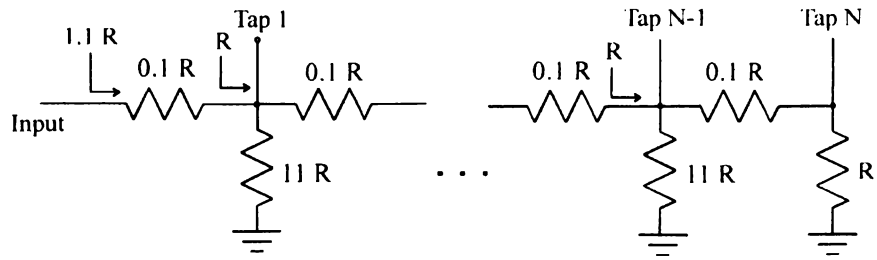


Fig.3.4 R-110R Ladder.

uator bandwidth and noise. The variation in the absolute resistance of the polysilicon layers that are available in the process used for this project is approximately ± 20%. Thus for an attenuator input resistance of 1 kΩ the termination resistance is R = (1000 ± 200) || 81 ≅ 75 ± 1.4 Ω which is a variation of approximately 2%. Larger values of input resistance would be desirable to reduce this variation, but would increase the noise contribution and lower the bandwidth of the attenuators. The R-110R ladder has an input resistance equal to 1.1 R requiring R > 900Ω for the desired 1 kΩ input resistance. The standard polysilicon resistance layer requires approximately 35 squares to achieve 900Ω, resulting in too much parasitic capacitance for the required bandwidth. The HR-poly layer requires approximately 1 square to achieve the 900Ω, and thus has much lower parasitic capacitance resulting in a higher bandwidth. A circuit based on a 1 square HR-poly unit cell with a width of 5 μm was used to generate an HSPICE simulation file. The NMOS transistor switches used to select the output tap and a behavioral model of the transconductor are included to provide loading of the taps. Each of the 0.1 R elements of the ladder is made of a parallel combination of 10 unit cells and the 11 R elements of the ladder are made of a

series combination of 11 unit cells. To improve the distributed nature of the modeling for AC simulations, each unit cell was approximated by five HSPICE wire models. Fig. 3.5 shows the AC response of this HR-poly R-110R attenuator using a 1V AC source. The simulated minimum bandwidth over the gain range is 290 MHz which is well above the targeted 150MHz. The delay dispersion was simulated using a transient simulation in which a –1V to +1V pulse was applied to the input of the attenuator and the zero cross of the output signal at the various taps was observed to determine the change in propagation delay for various gain settings. The simulation of the delay dispersion over the full gain range is shown in Fig. 3.6 and indicates a delay dispersion of 0.55 ns. This delay dispersion is less than the maximum permissible delay shift of 1.0ns and thus is acceptable. The estimated layout area required by the R-110R ladder is approximately 30,000 μ^2 The performance of the R-110R ladder appears acceptable, however, the use of the non-standard HR-poly resistors would make it more difficult to move the design to a new process, thus other approaches using the standard poly1 layer were investigated.

3.2.3 Preliminary Analysis of the Series/Parallel Attenuator

The series/parallel attenuator structure approximates the desired attenuator resistors using a series/parallel combination of unit resistors. The resistor combinations were selected by manually calculating the composite resistance and number of unit cells required to approximate a given desired resistor and selecting the configuration which results in the best trade-off between resistance approximation error and the number of unit cells used. The approximation error can be made arbitrarily small by using more resistors in the approximation, however, more resistors require larger layout areas and result in lower

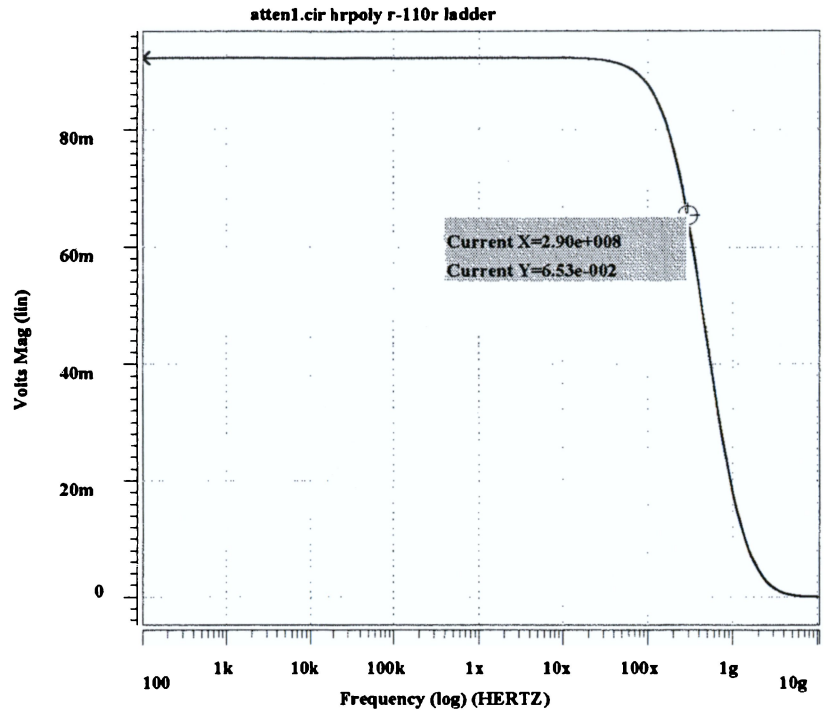


Fig.3.5 HR-poly R-110R Ladder Bandwidth Simulation.

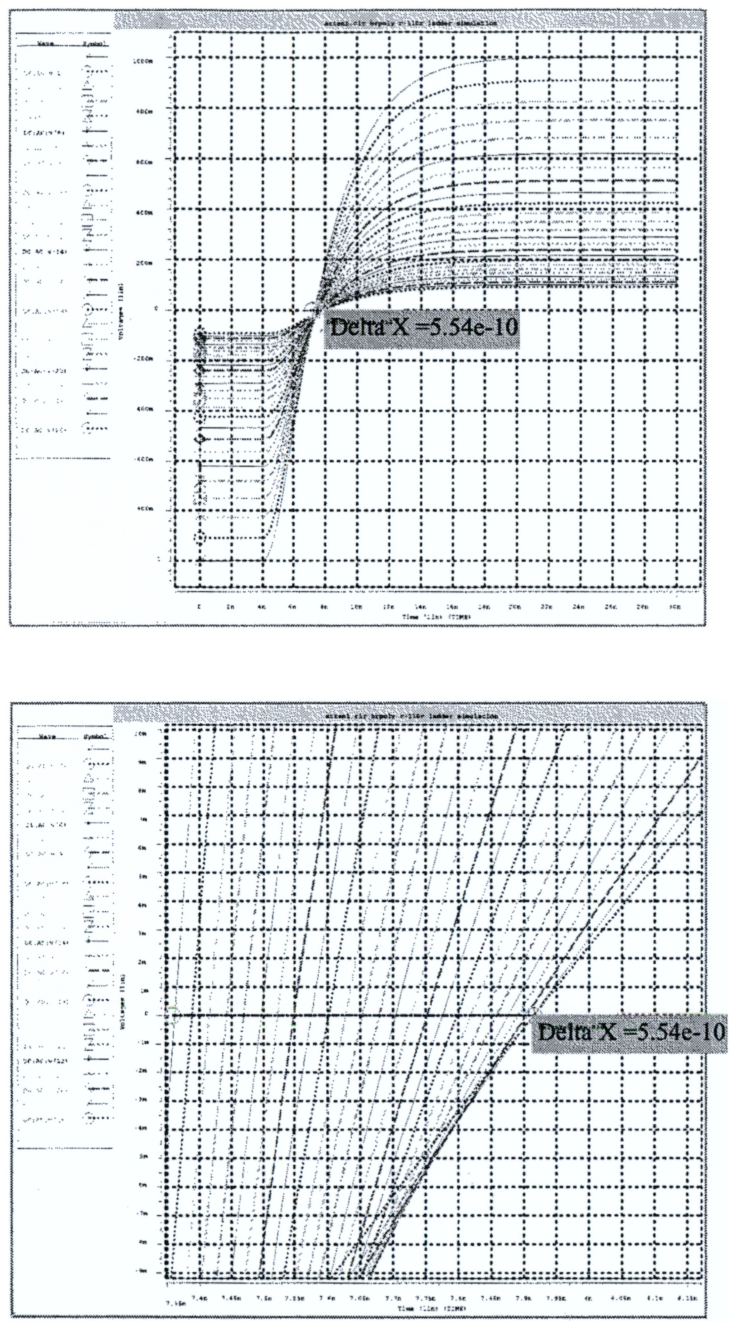


Fig.3.6 HR-poly R-110R Delay Dispersion Simulation with Close-up of Zero Crossings.

bandwidths due to larger parasitics. The resulting combinations for a 1 square unit cell are shown in Table 3.3 and result in the gain steps and gain errors shown in Table 3.4. The gain approximation errors for this approach can be as high as 7%.

The variation in total input resistance is higher for this approach because the contact resistance varies as much as 100% and is a non-negligible part of the unit cell resistance. For a 1 square unit cell, $R = 26 \pm 20\% + 10 + 100\%$ (or - 50%) $= 36 \pm 42\%$ which results in an input termination resistance of $R_{term} = 81 \,||\, (1000 \pm 420) = 75 \pm 2.2\%$. Thus the input termination is slightly less predictable with this architecture than for the R-110R ladder.

Simulations of the series/parallel attenuator are shown below. A circuit based on a 1 square unit cell with a width of 2.8 μm was used to generate the HSPICE simulation file. The NMOS transistor switches used to select the output tap and a behavioral model of the transconductor are included to provide loading of the taps. To improve the distributed nature of the modeling for AC simulations, each unit cell is approximated by five HSPICE wire models. Fig. 3.7 shows the AC response of this series/parallel attenuator using a 1V AC source. The simulated minimum bandwidth is 188 MHz which is above the targeted 150MHz. The delay dispersion was simulated using a transient simulation in which a –250 mV to +250 mV pulse was applied to the input of the attenuator and the zero cross of the output signal at the various taps was observed. The simulation of the delay dispersion over the gain range shown in Fig. 3.8 indicates a delay dispersion of 0.57 ns over the gain range, which is also acceptable. The attenuator layout with an enlarged view of the unit cell is shown in Fig. 3.9. The attenuator has a total area of approximately 33,000 μ^2.

Table 3.3: Series Parallel Combinations of a One-Square Unit Cell to Approximate the Desired Gain Steps

	r unit	r/2	r/3	r/4	r/5	r/6	r/7	# of unit cells	composite resistance
resistance	30	15	10	7.5	6	5	4.29		
r25	3							3	90
r24	2	1		1				8	82.5
r23	2	1						4	75
r22	2			1				6	67.5
r21	1	1	1	1				10	62.5
r20	1		2		1			12	56
r19	1	1			1			8	51
r18	1		1		1			9	46
r17	1			1		1		11	42.5
r16		1	1	1	1			14	38.5
r15	1					1		7	35
r14		1	1	1				9	32.5
r13			1	1	1	1		18	28.5
r12			2		1			11	26
r11			1	1	1			12	23.5
r10			1		2			13	22
r9			2					6	20
r8					3			15	18
r7			1		1			8	16
r6		1						2	15
r5				1	1			9	13.5
r4				1		1		10	12.5
r3					1	1		11	11
r2			1					3	10
r1						1	1	13	9.285714
r0	2	1	1	1				11	92.5
							total	243	

Table 3.4: Approximate Gain Steps for Series/Parallel Attenuator

resistor	resistance	cumula-tive	gain	%step err	approx. total gain	Theoreti-cal gain	abs. gain error	%Gain error
r25	90	996.78	1.10	0.68	11.45	10.83	0.62	5.74
r24	82.5	906.78	1.10	0.07	10.34	9.84	0.49	5.03
r23	75	824.29	1.10	0.09	9.41	8.95	0.46	5.11
r22	67.5	749.29	1.11	0.91	8.56	8.14	0.42	5.20
r21	62.5	681.79	1.10	0.84	7.72	7.41	0.32	4.25
r20	56	619.29	1.11	0.53	7.07	6.73	0.34	5.12
r19	51	563.29	1.10	0.41	6.40	6.12	0.28	4.56
r18	46	512.29	1.11	1.24	5.79	5.56	0.23	4.14
r17	42.5	466.29	1.10	0.26	5.20	5.05	0.14	2.86
r16	38.5	423.79	1.10	0.07	4.74	4.59	0.14	3.13
r15	35	385.29	1.10	0.07	4.31	4.18	0.13	3.06
r14	32.5	350.29	1.08	2.02	3.91	3.80	0.11	2.98
r13	28.5	317.79	1.12	1.37	3.63	3.45	0.18	5.10
r12	26	289.29	1.11	1.15	3.25	3.14	0.12	3.69
r11	23.5	263.29	1.12	1.85	2.92	2.85	0.07	2.51
r10	22	239.79	1.09	0.91	2.61	2.59	0.02	0.65
r9	20	217.79	1.09	1.01	2.40	2.36	0.04	1.58
r8	18	197.79	1.10	0.11	2.20	2.14	0.06	2.61
r7	16	179.79	1.12	2.15	2.00	1.95	0.05	2.72
r6	15	163.79	1.09	0.74	1.78	1.77	0.01	0.56
r5	13.5	148.79	1.10	0.19	1.63	1.61	0.02	1.30
r4	12.5	135.29	1.08	1.61	1.48	1.46	0.02	1.11
r3	11	122.79	1.12	1.48	1.37	1.33	0.04	2.76
r2	10	111.79	1.12	1.62	1.23	1.21	0.02	1.27
r1	9.29	101.79	1.10	0.35	1.10	1.1	0.00	0.35
r0	92.50	92.50	1		1	1	0	0

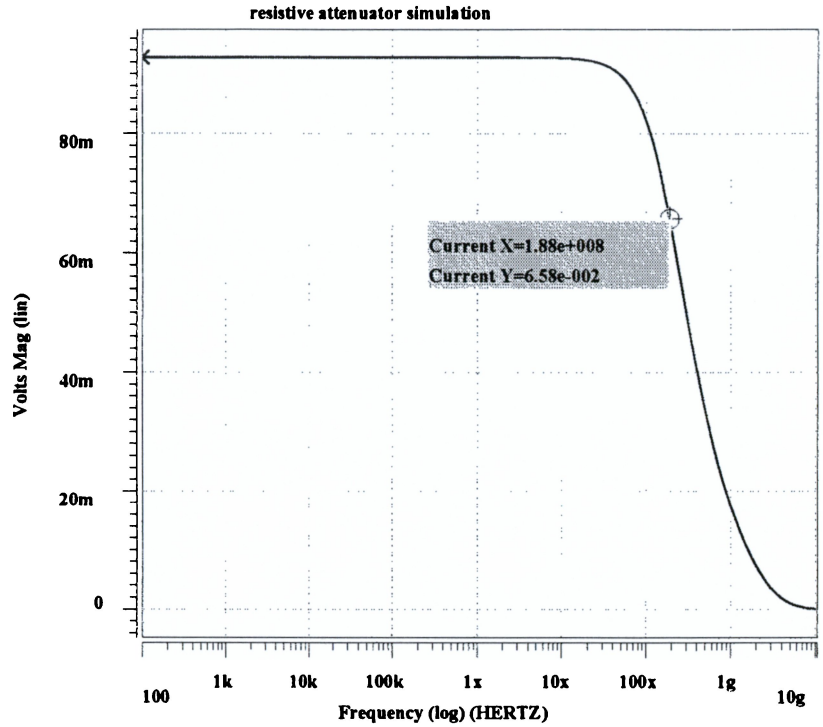


Fig.3.7 Bandwidth Simulation for Series/Parallel Ladder.

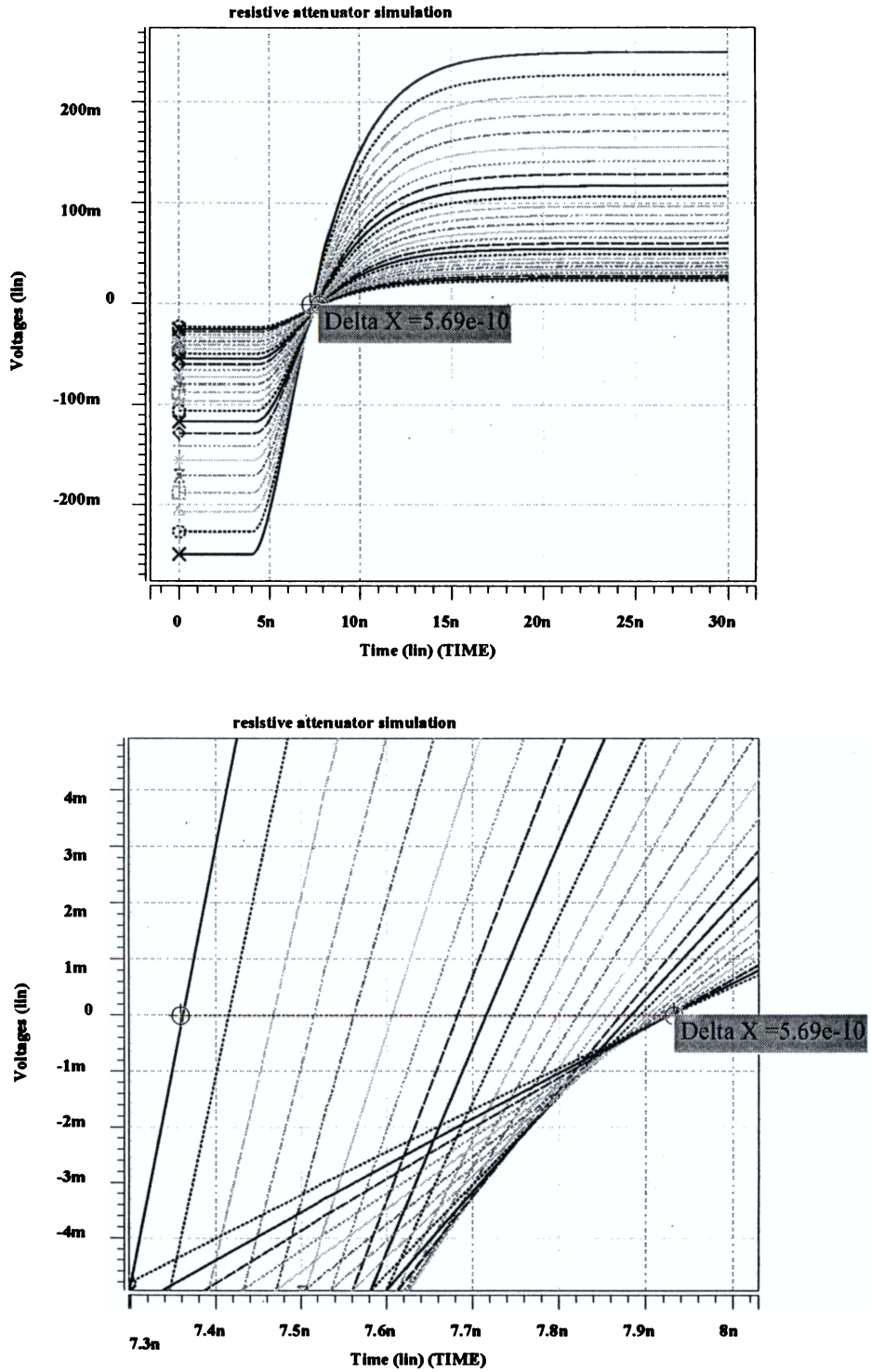


Fig.3.8 Delay Dispersion Simulation for Series/Parallel Ladder with Close-up of Zero Crossings.

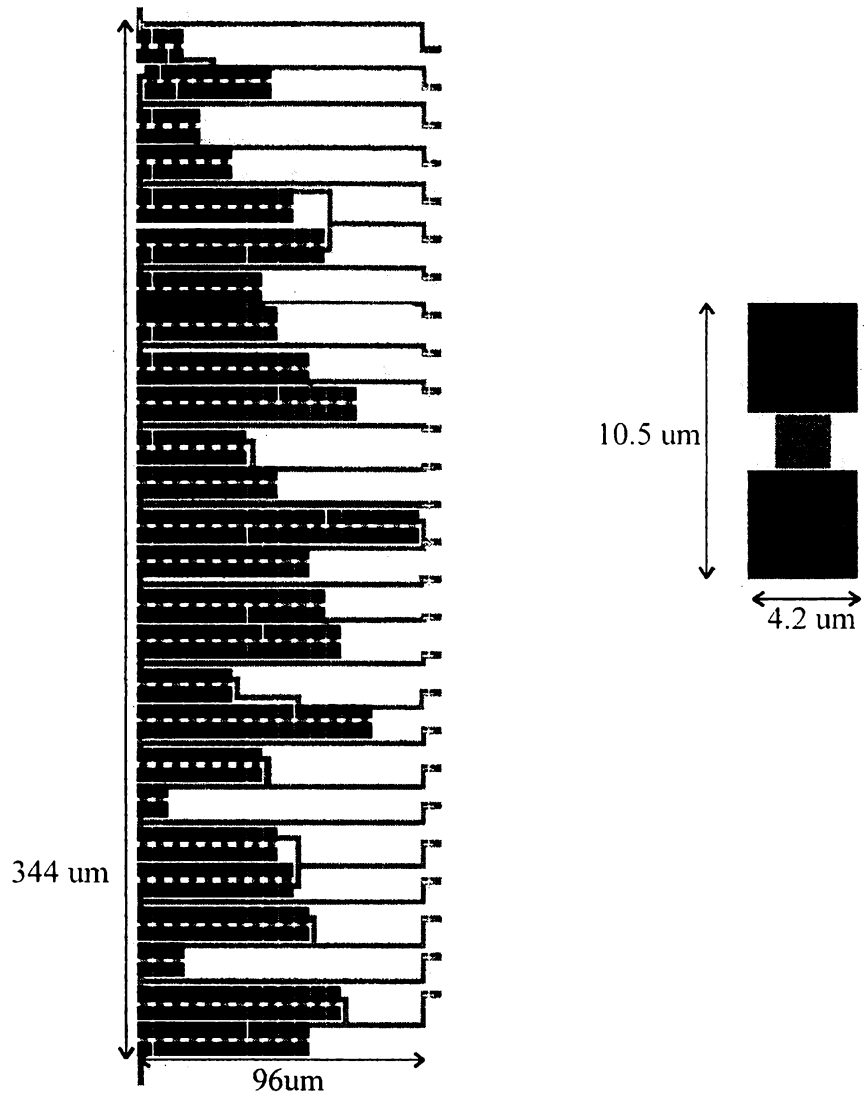


Fig.3.9 Layout of Series/Parallel Ladder and Close Up of Unit Cell .

3.2.4 Preliminary Analysis of the Tapped Resistor Attenuator

The tapped resistor attenuator approximates the desired resistors using an integer number of unit resistors with no contacts on the ends. This approach eliminates the minimum number of squares constraint because there are no contacts to contribute to the total resistance of the unit cell. The choice of such a unit cell results in a continuous polysilicon resistor with many taps along the side. The number of unit cells was chosen to approximate the gain steps within ± 2% by calculating the maximum gain step error and rms gain step error for a number of total unit cells ranging from 98 to 450. The choice of 293 unit cells provides the best trade off between gain step error and required area. To significantly reduce the gain step error would require increasing the number of unit cells to 421, which would require approximately 44% more area. Table 3.5 contains the number of unit cells per tap and the resulting gains and gain errors for the 293 unit cell ladder. The variation in the absolute resistance of the polysilicon layer is ± 20%. Thus for a 1 kΩ input resistance the variation in the 75 Ω termination resistance R is given by R = 81 || (1000 ± 200) or approximately 75 ± 2%. The layout size of the unit cell is determined by the minimum height allowed by the design rules of the process and the desired input resistance. The minimum height for the unit cell is determined by the minimum permissible distance between the metal 1 contacts on the unit cells and the minimum size of the contacts. The minimum size for a contact in this process using SCMOS design rules is 4 lambda, where lambda = 0.35 microns. The minimum spacing between contacts is also 4 lambda resulting in an 8 lambda high unit cell. For a 1kΩ input resistance and 293 unit cells, the unit cell must be 0.131 squares. Thus the unit cell is 8 lambda (2.8 μm) high by 61 lambda (21.35 μm) wide.

Table 3.5: Unit Cells per Tap, Gains, and Gain Errors for the Tapped Resistor Attenuator

Resis-tor	# of cells	Gain Step	Abs. step error	% step error	total gain		Abs. gain error	% gain error
RIN total	293				Approxi-mate	Theoreti-cal		
R25	27	1.10	0.00	0.14	10.85	10.83	0.02	0.16
R24	24	1.10	0.00	0.08	9.85	9.85	0.00	0.02
R23	22	1.1	0	0.00	8.96	8.95	0.01	0.10
R22	20	1.1	0	0.00	8.15	8.14	0.01	0.10
R21	18	1.10	0.00	0.10	7.41	7.40	0.01	0.10
R20	17	1.10	0.00	0.28	6.74	6.73	0.01	0.20
R19	15	1.1	0	0.00	6.11	6.12	0.00	0.08
R18	14	1.10	0.00	0.27	5.56	5.56	0.00	0.08
R17	12	1.10	0.00	0.29	5.04	5.05	0.02	0.34
R16	11	1.10	0.00	0.24	4.59	4.59	0.00	0.05
R15	10	1.10	0.00	0.26	4.19	4.18	0.01	0.19
R14	9	1.10	0.00	0.39	3.81	3.80	0.02	0.46
R13	9	1.11	0.01	0.53	3.48	3.45	0.03	0.85
R12	8	1.10	0.00	0.35	3.15	3.14	0.01	0.31
R11	7	1.1	0	0.00	2.85	2.85	0.00	0.04
R10	6	1.09	0.01	0.57	2.59	2.59	0.00	0.04
R9	6	1.10	0.00	0.31	2.37	2.36	0.01	0.53
R8	5	1.09	0.01	0.51	2.15	2.14	0.00	0.21
R7	5	1.10	0.00	0.38	1.96	1.95	0.01	0.73
R6	4	1.09	0.01	0.83	1.78	1.77	0.01	0.35
R5	4	1.1	0	0.00	1.63	1.61	0.02	1.19
R4	4	1.11	0.01	1.01	1.48	1.46	0.02	1.19
R3	3	1.09	0.01	0.83	1.33	1.33	0.00	0.18
R2	3	1.1	0	0.00	1.22	1.21	0.01	1.01
R1	3	1.11	0.01	1.01	1.11	1.1	0.01	1.01
R0	27				1	1	0.00	0.00

Simulations of this configuration are shown below. A circuit based on this unit cell was used to generate the HSPICE simulation file. The NMOS transistor switches used to select the output tap and a behavioral model of the transconductor were included to provide loading of the taps. To improve the distributed nature of the modeling for AC simulations, each unit cell was approximated by five HSPICE wire models. The simulated AC response with a bandwidth of approximately 217 MHz is shown in Fig. 3.10. The simulated delay dispersion over the gain range of approximately 824 as is shown in Fig. 3.11. The bandwidth is well over the required 100MHz and the dispersion is within the required 1ns. An enlarged view of the lower portion of the resulting attenuator structure is shown in Fig. 3.12. The attenuator consists of 293 unit cells with a total area of 19,400 μ^2.

3.2.5 Comparison of Attenuator Architectures

Both of the series attenuators discussed above have the potential to meet the requirements for the Phase II design. The tapped polysilicon resistor appears to be the better choice because it avoids many of the contact issues associated with the series/parallel ladder, has much smaller gain errors, and requires only 60% of the area needed for the series/parallel ladder. However, the polysilicon strip structure is more complicated to correctly model because the resulting structure lacks symmetry. The resistor structures used in the series/parallel ladder are symmetric in all but one dimension, thus the 1-dimensional model used by HSPICE provides a reasonably good model. The lack of symmetry in the polysilicon strip structure adds some doubt as to the validity of using a 1-dimensional model. The tapped polysilicon resistor was chosen as the preferred attenuator, however, the series/parallel attenuator was also fabricated on the prototype 1 chip to provide a

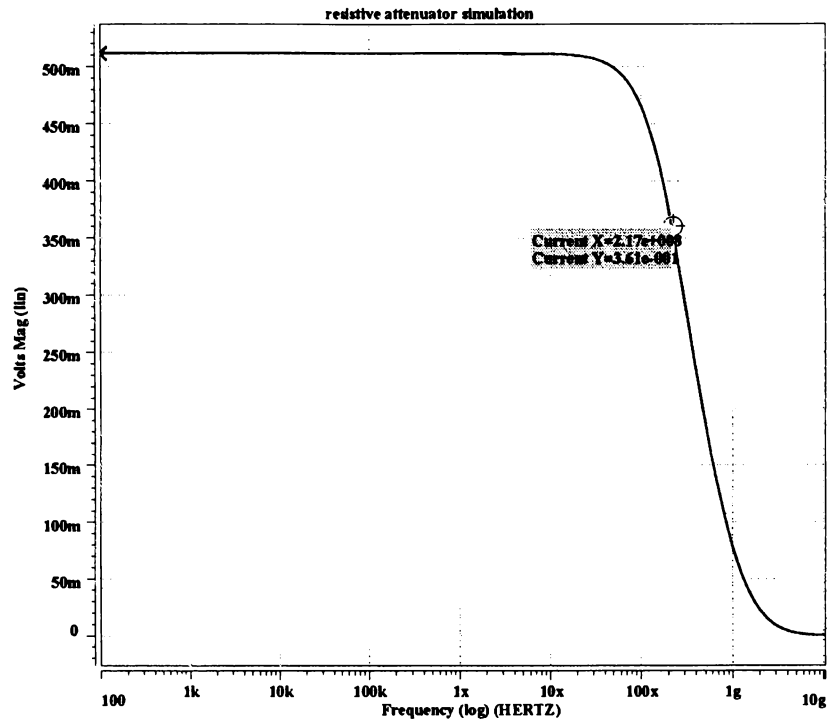


Fig.3.10 Bandwidth Simulation for Tapped Resistor Attenuator.

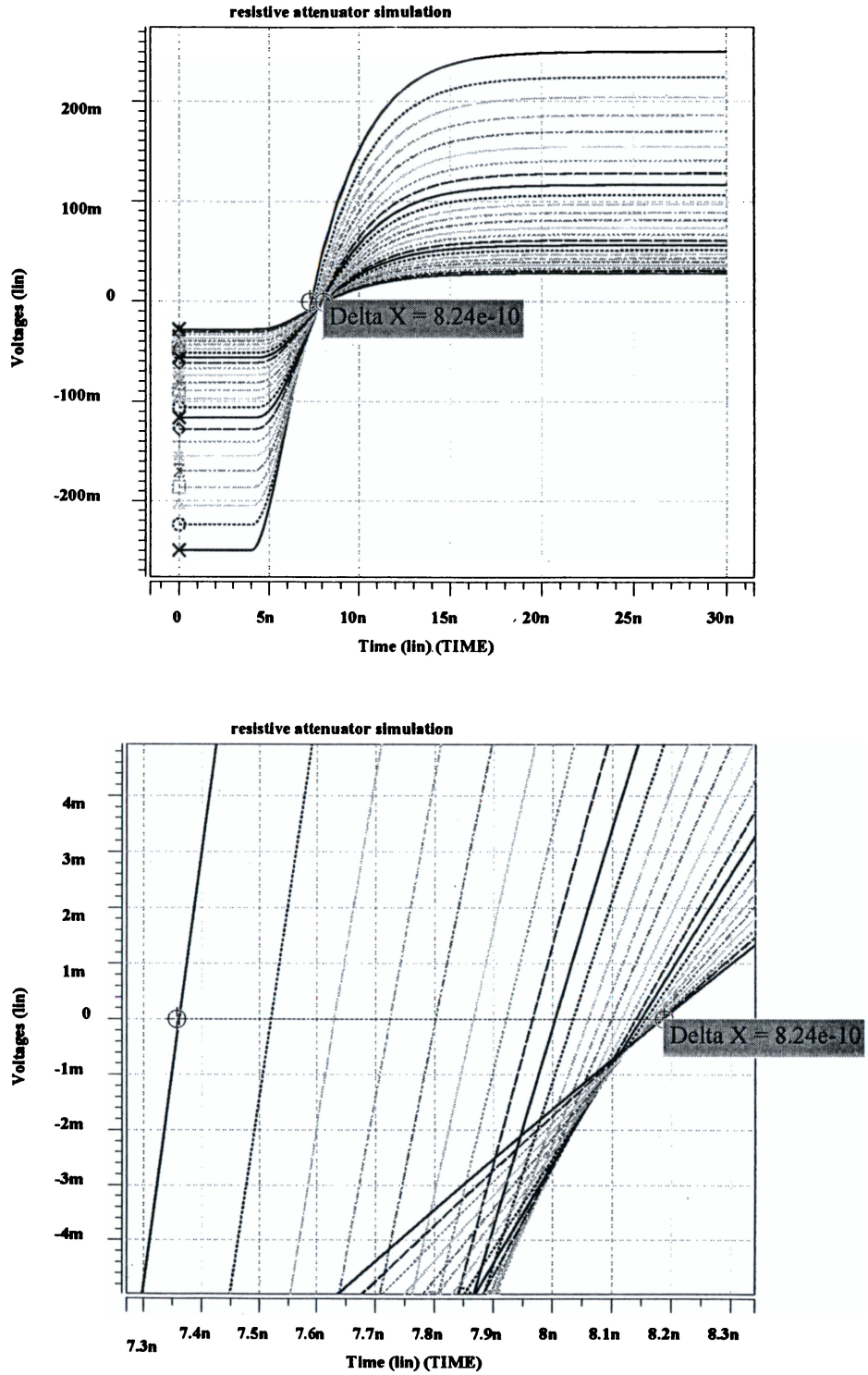


Fig.3.11 Delay Dispersion Simulation for Tapped Resistor Attenuator with Close-up of Zero Crossings.

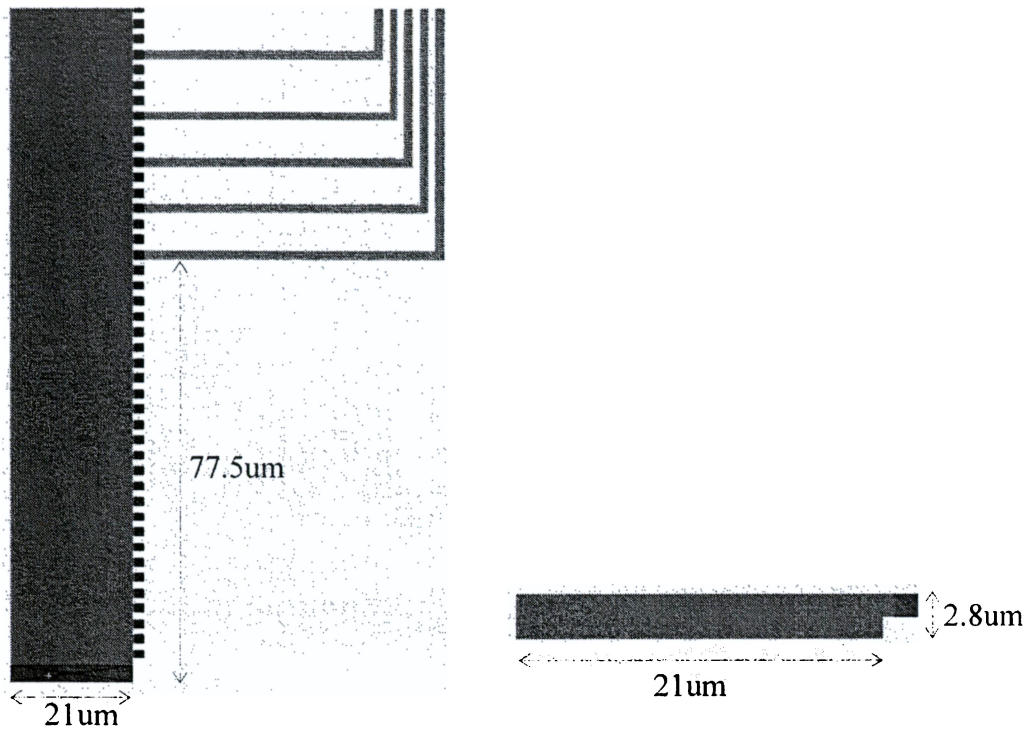


Fig.3.12 Tapped Resistor Attenuator (Bottom 5 taps Shown) and Polysilicon Unit Cell (enlarged).

backup in the event that the performance of the tapped polysilicon resistor was not acceptable.

3.2.6 Additional Analysis of the Tapped Resistor Attenuator

Simulations for the Second Version of the Tapped Resistor Attenuator

For the second prototype, the tapped resistor attenuator was modified to allow the dimensions of the resistor to be reduced by a factor of 2. The length of the original unit cell was required to be at least 8 lambda so that the 4 lambda long taps could be separated by 4 lambda when the unit cells were arrayed. The new layout removes the unused taps allowing a smaller unit cell length. The reduced unit cell which is 4 lambda long by 30

lambda wide was used to generate an HSPICE simulation file. The NMOS transistor switches used to select the output tap and a behavioral model of the transconductor are included to provide loading of the taps. To improve the distributed nature of the modeling for AC simulations, each unit cell is approximated by five HSPICE wire models. NMOS gain-select switches were included at each tap and a behavioral model of the transconductor including input capacitance was used to model the loading of the taps. Fig. 3.13 shows the AC response of this series/parallel attenuator using a 1V AC source. The simulated minimum bandwidth is 311 MHz which is well above the targeted 150MHz. The delay dispersion was simulated using a transient simulation in which a –250mV to +250mV pulse was applied to the input of the attenuator and the zero cross of the output signal at the various taps was observed. The simulation of the delay dispersion over the gain range shown in Fig. 3.14 indicates a delay dispersion of 380 ps over the gain range, which is less than the allowed delay variation of 1 ns.

Attenuator Noise Calculations

The noise associated with the attenuator resistors and the NMOS gain-select switches is calculated as,

$$\sqrt{4ktT(R_{thev} + R_{on})},$$

where R_{thev} is the Thevenin equivalent resistance for the associated tap and R_{on} is the switch on resistance. The input referred noise is plotted in Fig. 3.15 as a function of gain setting. The input referred noise level increases for lower gain settings where the signal amplitude is largest resulting in a relatively constant Signal to Noise Ratio (SNR) over the gain range.

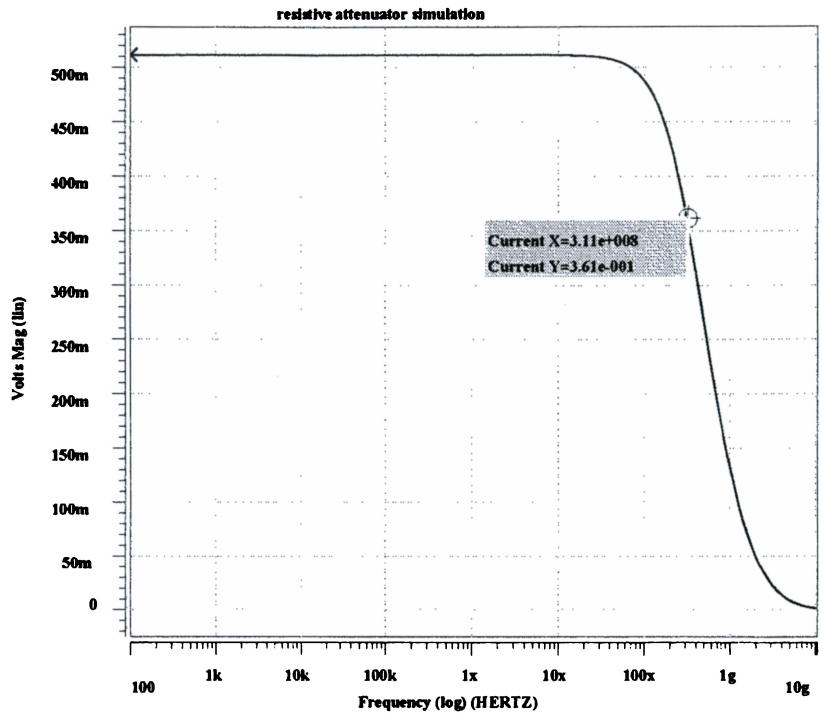


Fig.3.13 Bandwidth Simulation for Small Tapped Resistor Attenuator.

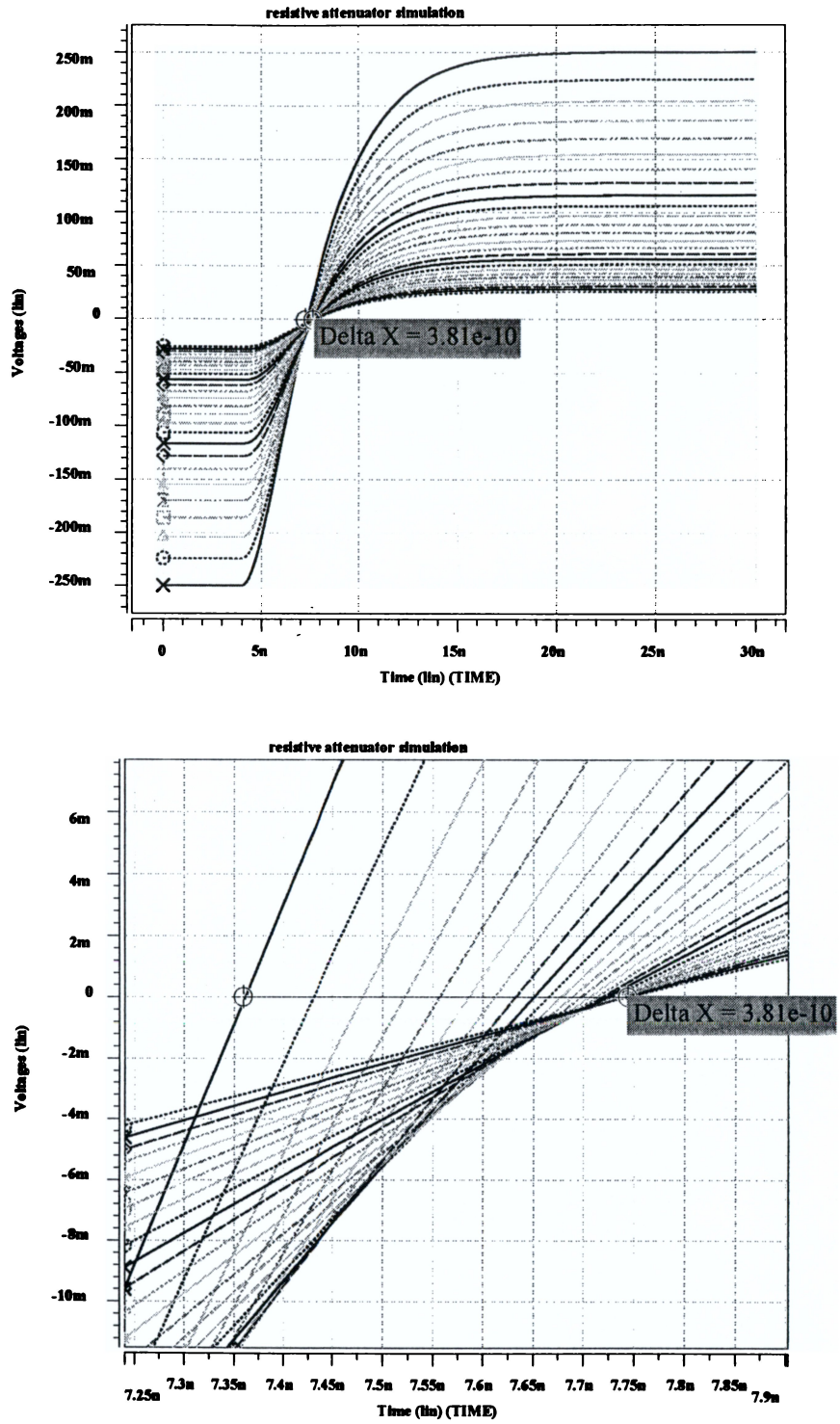


Fig.3.14 Delay Dispersion Simulation for Small Tapped Resistor Attenuator with Close-up of Zero Crossings.

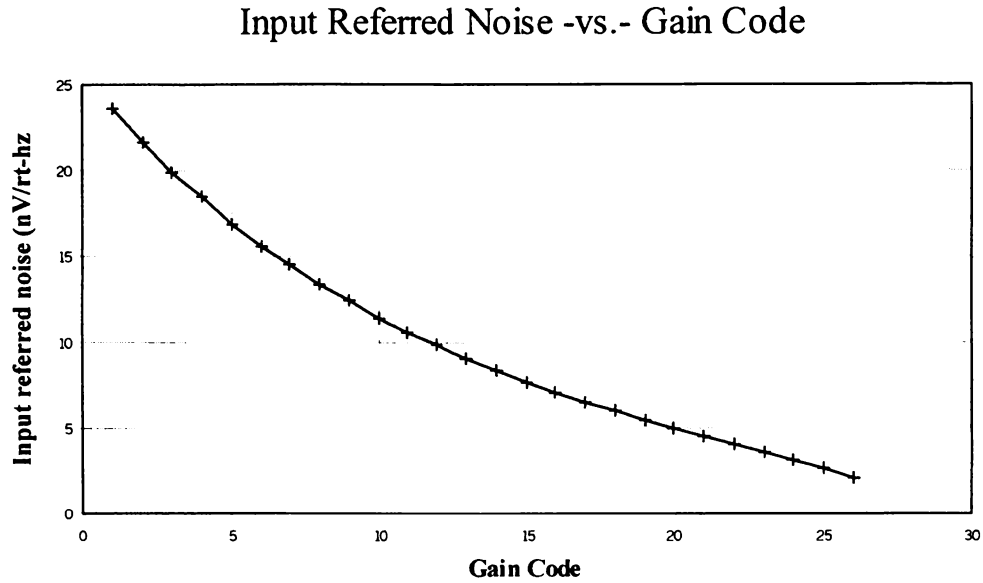


Fig.3.15 Attenuator Noise Calculations.

Delay Dispersion Analysis

The preliminary modeling of the delay dispersion for the attenuators using HSPICE discussed above suggests a monotonic delay variation as a function of gain. A simple hand calculation was performed to further investigate the characteristics of the delay. The results of the hand calculation using a single pole determined by the Thevenin output resistance of the attenuator taps and a fixed load capacitance is shown in Fig. 3.16 and has a nearly parabolic relation to gain. The delay characteristics were further studied by simulation using the post-layout circuit extraction of the VGA channel combined with the distributed model of the attenuator. The post-layout simulation through the VGA channel is shown in Fig. 3.17 and exhibits a combination of the two relations above. The delay in lowest for maximum gain and increases as the attenuation increases up to a maximum

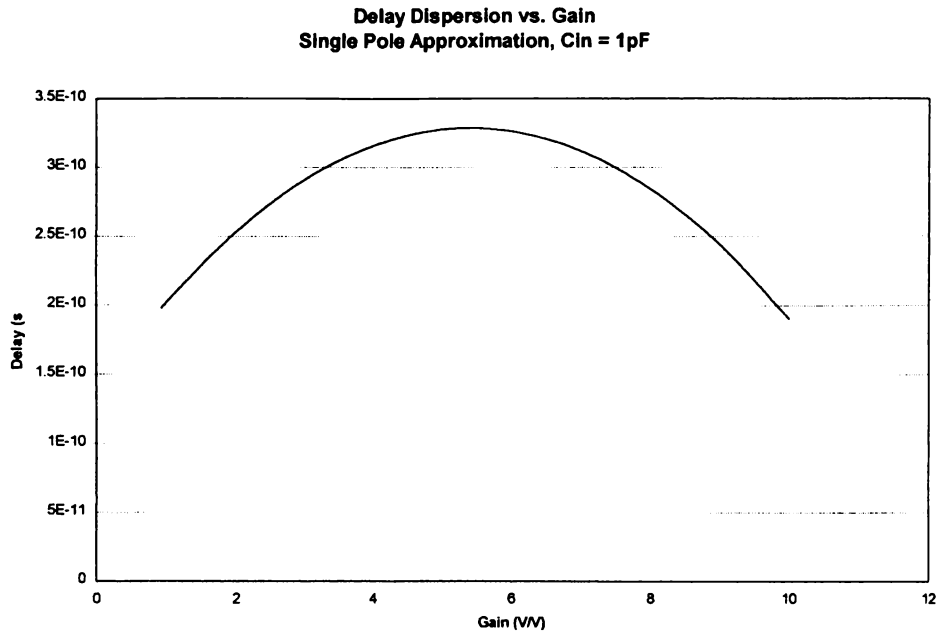


Fig.3.16 1st Order Delay Dispersion Calculation.

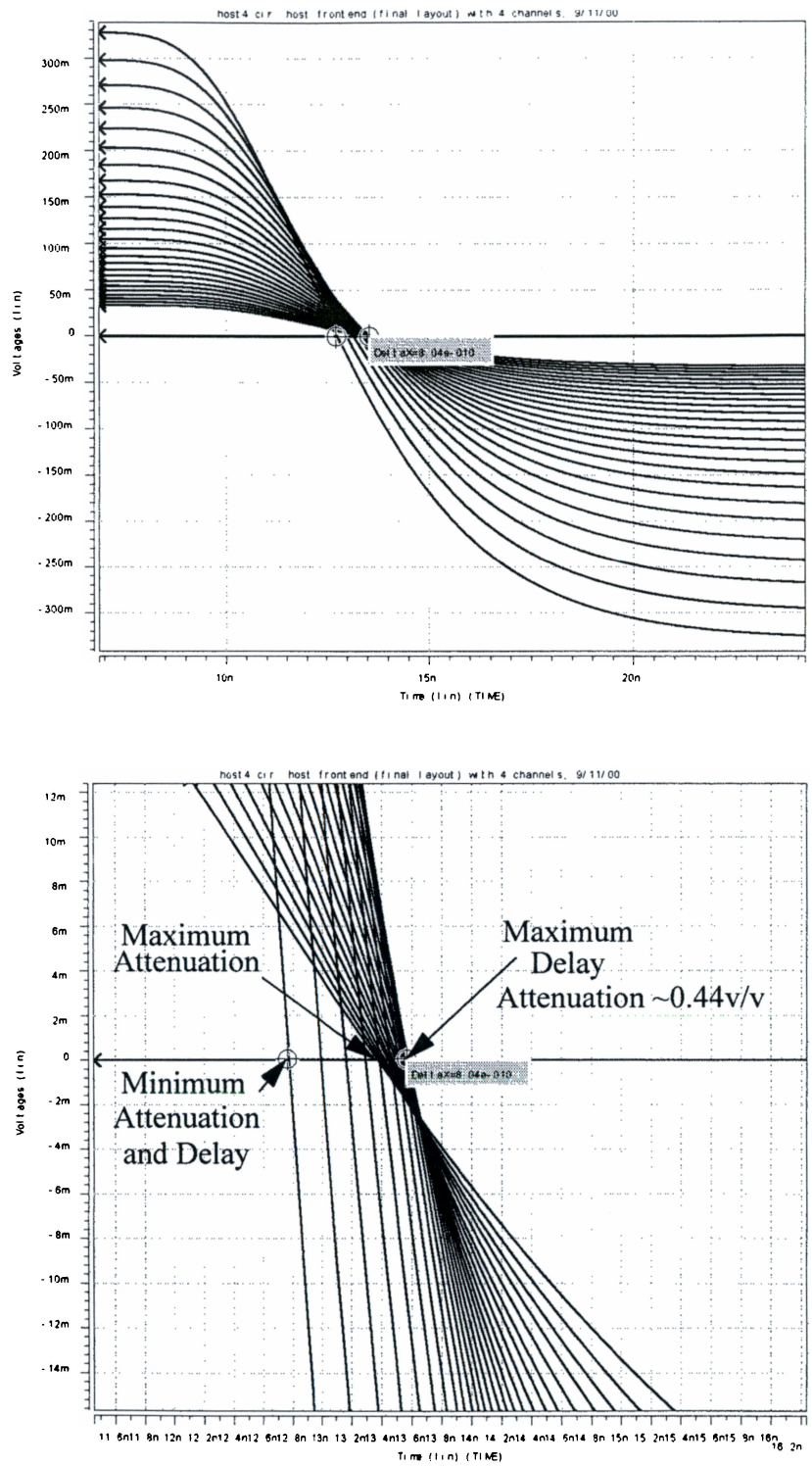


Fig.3.17 Full Channel Delay Dispersion from Post-Layout Simulation.

delay of approximately 800 ps, the delay then decreases as the attenuation increases further. This more complicated relation exhibited by the post layout simulation better reflects the experimental results and is probably due to the more accurate modeling of the loading of the taps provided by the post-layout extraction of the transconductor circuit.

3.3 Transconductor

The purpose of the differential transconductor is to perform a voltage to current conversion. The transconductance (Gm) of the transconductor is defined as the rate of change of the differential output current (Iout) with respect to the differential input voltage (Vin) or

$$Gm = \frac{dI_{out}}{dV_{in}} \approx \frac{\Delta Iout}{\Delta Vin}.$$

The transconductor performs the voltage-to-current conversion necessary to provide a current output from a voltage input.

3.3.1 Transconductor Design Issues and Selection

Primary Transconductor Performance Issues

The primary performance issues for the transconductor are transconductance, linearity, bandwidth, and noise performance. The Phase 2 chip has the additional requirement that the common mode input range include ground. For a tuned transconductor, other important issues are offset, the tuning current range, and the variation in the common mode output level due to tuning. The transconductance must be predictable and stable to produce a well controlled gain. The circuit must be reasonably linear over the range of signal input amplitudes. The bandwidth of the transconductor should be approximately 150 MHz to

allow a system bandwidth of 100 MHz. The transconductor to a large degree dominates the noise of the entire system, thus a low noise transconductor design is essential. For tuned transconductors, offsets in the tuning loop can result in gain errors, and the tuning range affects how well the feedback loop can correct for processing and temperature variations. Additionally, the common mode output level should be held relatively constant to maintain the dynamic range and correct operation of circuits following the VGA.

Transconductor Types

Several transconductor designs were considered for the project including resistor based transconductors, differential pairs, and linearized differential pairs.

Resistor Based Transconductors

Resistor based transconductors use a resistive element, which can be a passive resistor or an ohmic mosfet, to perform the voltage to current conversion. They typically utilize some sort of buffer to apply the input voltage to the resistive element while maintaining high input impedance. Some examples of this type of transconductor can be found in [24, 46]. Fig. 3.18 shows a typical configuration using a passive resistor. The differential output current for the transconductor in Fig. 3.18 is given by

$$I_{o1(differential)} = 2(\frac{V_i}{R_E})$$

This type of transconductor has very good linearity, and moderate bandwidth, but usually has higher noise because the noise of the buffers adds directly to the thermal noise of the resistor. Also, the buffers often have two input devices and use feedback to give good

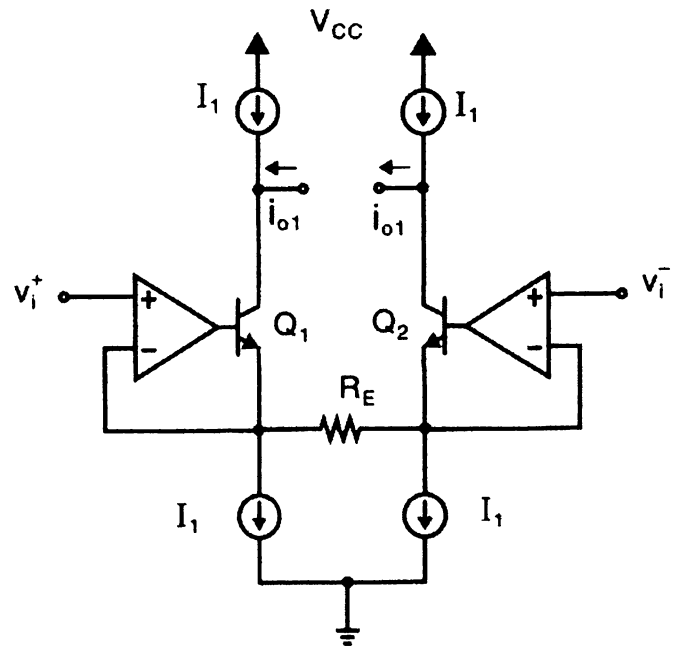


Fig.3.18 Resistor Based Transconductor [24].

accuracy, thus for a differential transconductor there are usually four input transistors contributing noise.

Differential Pair Transconductor

Probably the simplest differential transconductor is the differential pair. The size of the devices and the tail current can be used to set the nominal transconductance of the pair, but a tuning scheme is needed to maintain a well-controlled transconductance over process and temperature variations. The noise of the differential pair is usually the lowest and the bandwidth highest of the transconductors discussed here, primarily due to the simplicity of the circuit. The linear region for the differential pair is small. However, for the present

application the signal at the input of the transconductor is in the 50mV range so that the limited linearity is not a major deficiency.

Linearized Differential Pair Transconductor

Many approaches have been taken to improve the linearity of the differential pair [12, 47-53]. These approaches are typically only helpful if linearity is a dominant design issue, otherwise, they only increase the noise and complexity of the design and decrease the bandwidth. Given the noise and bandwidth requirements for the Phase II design, and the small signal level at the input of the transconductor, linearizing the differential pair is of secondary interest and will only degrade the bandwidth and noise performance.

Tuned Differential Pair Transconductor

The transconductance of a differential pair for a given bias current is highly dependent on processing variations and temperature. Thus, the transconductance must be regulated to produce a predictable gain over process and temperature variations. This regulation is often done automatically using a feedback circuit to set the bias current in the differential pair to a level that produces the desired transconductance.

Fig. 3.19. shows one approach to tuning the transconductance to $1/R_{tune}$ for a given resistor (R_{tune}) using an externally supplied reference current (I_{ref}). I_{ref} is duplicated by a two output current mirror to produce I_{tune} and I_{off}. I_{tune} flows through R_{tune} to produce a reference voltage $V_{tune} = I_{tune}R_{tune}$ across the input of the transconductor. I_{off} is added to one of the differential current outputs of the transconductor to produce an offset current. One of the outputs is then inverted using a current mirror and then added to the other output to produce a single-ended output current that is equal to the differential output of the

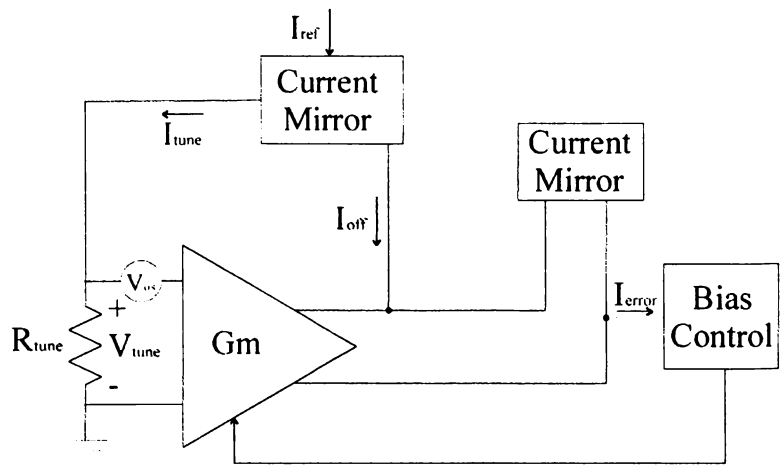


Fig.3.19 Transconductor Tuning Circuit.

transconductor minus the offset current I_{off}. The feedback circuit uses this single-ended output as the error signal and adjusts the transconductor bias current to set the error signal to zero. This occurs when the transconductor differential output exactly cancels I_{off} and the transconductance is equal to

$$G_m = \frac{I_{off}}{V_{tune}} = \frac{I_{off}}{I_{tune}R_{tune}} = \frac{I_{ref}}{I_{ref}R_{tune}} = \frac{1}{R_{tune}}.$$

Transconductor offset (V_{os}) is a source of tuning error because it adds directly to V_{tune}. The resulting transconductance in the presence of an offset is given by

$$G_m = \frac{I_{off}}{V_{tune} + V_{os}} = \frac{I_{off}}{I_{tune}R_{tune} + V_{os}} = \frac{I_{ref}}{I_{ref}R_{tune} + V_{os}} = \frac{1}{R_{tune} + \frac{V_{os}}{I_{ref}}}.$$

Thus, accurate tuning requires a low transconductor offset voltage.

A typical approach for tuning multiple transconductors on the same chip is to use a master – slave configuration. The master transconductor is used in a tuning loop as described above to establish a transconductor bias level that produces the desired transconductance. The bias level established in the master is replicated in the slave

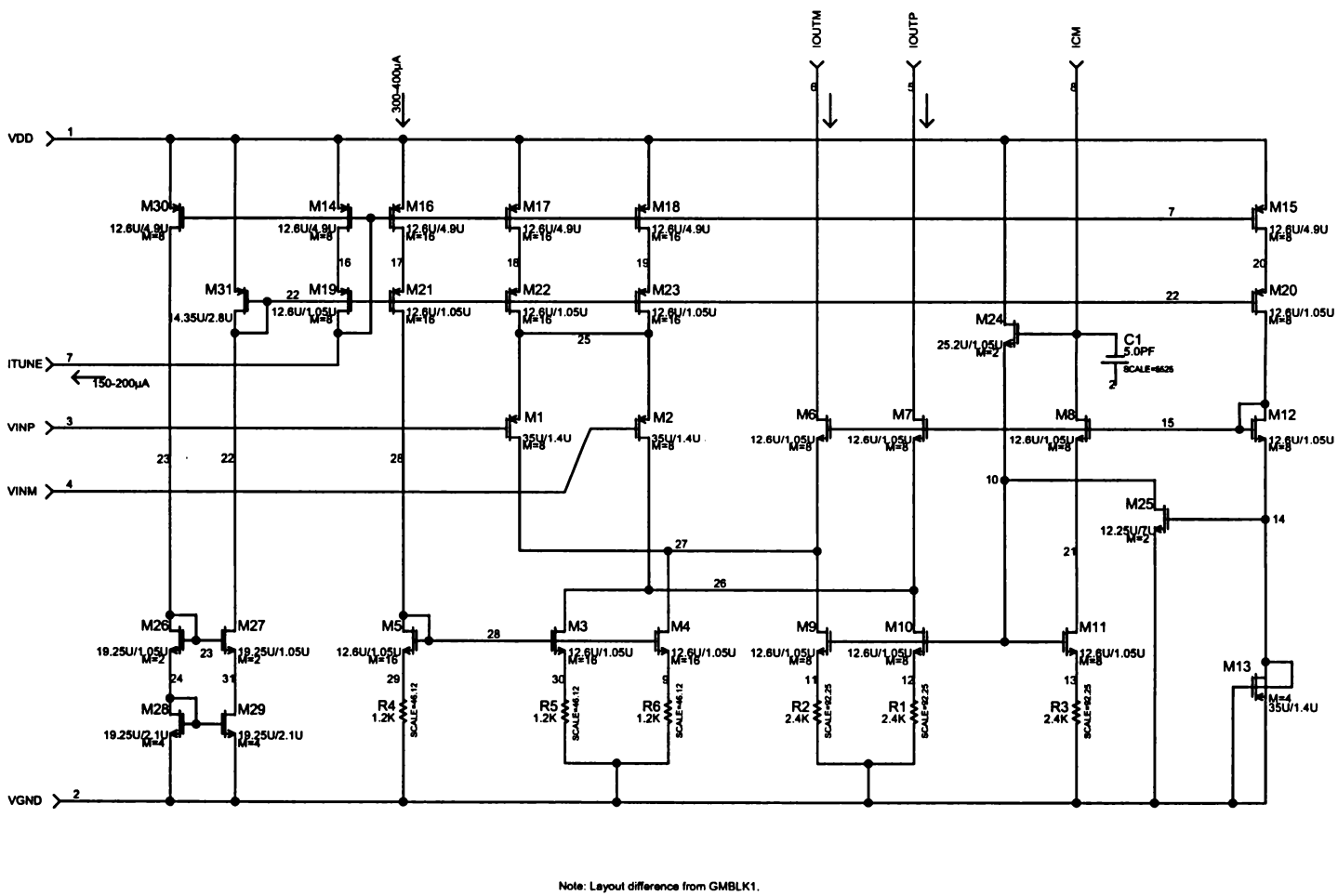
transconductors that are used in the signal path. Matching between the master and the slave transconductor is critical and thus the slave transconductors are physically designed as exact duplicates of the master. Mismatch in the transistors or bias current between the master and the slaves produces transconductance errors in the slaves and thus must be minimized.

Transconductor Survey Summary

Due to the noise, bandwidth, and linearity requirements for the transconductor stage of the Phase II VGA, the tuned differential pair using a master – slave tuning scheme appears to be the optimum choice and has been designed for fabrication on a prototype chip. All of the more complicated designs that were considered have inferior noise and bandwidth performance compared to the differential pair without necessarily offering any performance improvements relevant to this application.

3.3.2 Design of the Tuned-Differential-Pair, Folded-Cascode Transconductor

The transconductor stage shown in Fig. 3.20 consists of an input stage based on a tuned PMOS differential pair followed by a folded cascode output stage. The input pair consists of M1 and M2 with a tuned tail current supplied by transistors M17,M18, M22, and M23. The current sources composed of M3, M4, R5, and R6 are set to match the tuning current and thus produce a zero common mode level at the output of the differential pair. The constant current sources composed of M9, M10, R1, and R2 re-establish a CM current level in the output stage that is to first order independent of the tuning current. Transistors M6 and M7 are cascode devices and form a folded cascode output for the transconductor.



Note: Layout difference from GMBLK1.

Fig.3.20 GMBLK2 Schematic.

Design of the Differential Pair

A design methodology presented in [54] was used in the selection of the differential pair. This methodology is based on the use of the Inversion Coefficient (IC) which indicates the level of inversion in the channel of the MOSFET and readily identifies the region of operation of the transistor. IC is defined as

$$IC = \frac{I_D}{I_0\left(\frac{W}{L}\right)}$$

where (W/L) is the aspect ratio of the transistor, I_D is the drain current and, $I_0 = 2nkU_T^2$ is the normalization current. I_0 is process dependent and is equal to the drain current of a unity aspect ratio transistor at the center of moderate inversion (IC = 1). The transistor is in weak inversion for IC < 0.1, moderate inversion for 0.1 < IC < 10, and strong inversion for IC > 10.

The ratio of transconductance to drain current called transconductance efficiency is a function of IC and is given by

$$G_m/I_D = (1/[nU_T(\sqrt{0.25 + IC} + 0.5)])$$

where n is the slope factor, U_T is the thermal voltage kT/q [54]. The simulated transconductor efficiency for the process used in this project is plotted verses IC in Fig. 3.21. The efficiency is highest in weak inversion and decreases monotonically as the region of operation moves toward strong inversion. Thus for a given drain current the highest transconductance can be obtained by biasing the transistor in weak inversion.

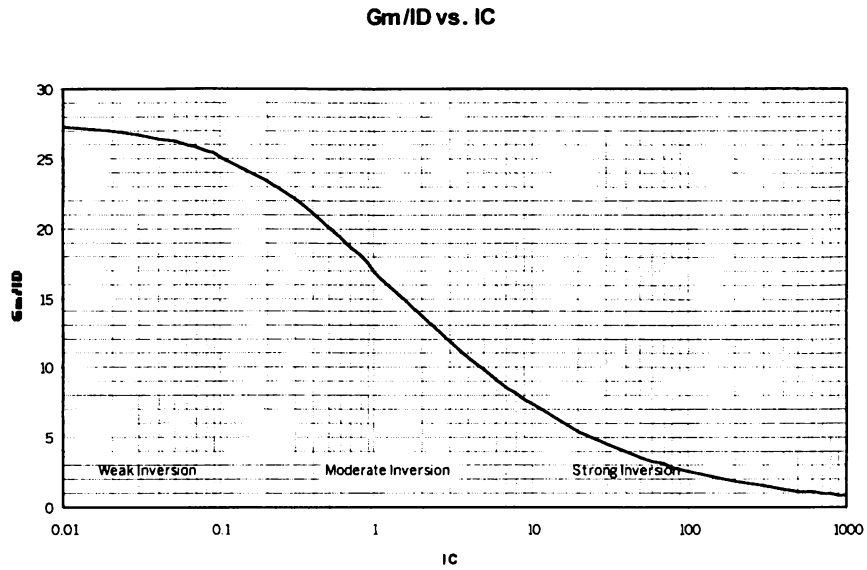


Fig.3.21 Transconductance Efficiency as a Function of IC.

The transconductance of 2 mS (1/500 ohm) was chosen to be well below the targeted noise level to allow the total noise of the channel to still be within the targeted noise range when the noise of the other circuits in the channel are added. The input pair is required to be a PMOS pair because the input common mode range includes ground. The region of operation for the transistors in the input pair was chosen based on a trade off between linearity, the desired bias current, and the saturation voltage Vdsat. A 2 mS transconductance and a drain current of 350uA imply a transconductance efficiency ratio of approximately 5.7, thus, the differential pair is biased in strong inversion with an inversion coefficient of approximately 19 based on the curve in Fig. 3.21. Fig. 3.22 contains a plot of the input voltage corresponding to a 1-dB compression in the differential output current vs. IC for a differential pair biased for a constant transconductance of 2 mS. The data points in the plot were extracted from multiple transient simulations performed at different levels of inver-

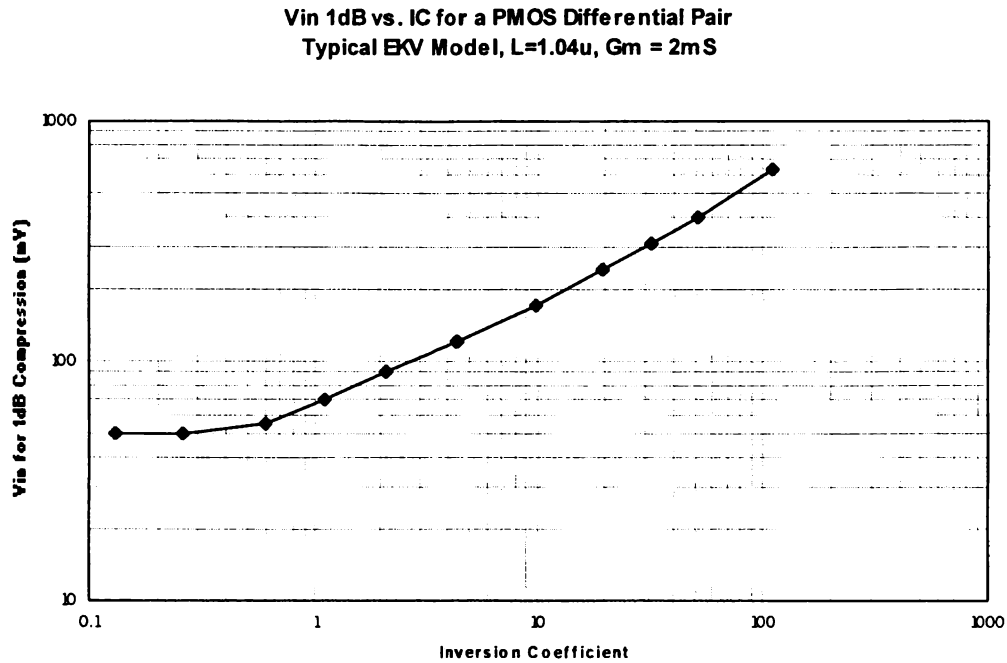


Fig.3.22 Simulated Input Pair Linearity as a Function of IC, for constant Gm = 2mS

sion in the input pair. In each transient simulation the bias current for the differential pair is established using a feedback loop to set the transconductance to 2 mS, then the input differential voltage is swept from 0 to 1v and the output differential current is examined to determine the 1 dB compression point. Equation 3.128 from [12] shown below, gives the differential output current as a function of differential input voltage for MOS transistors in strong inversion.

$$\Delta I_d = \mu_n \frac{C_{ox} W}{2L} V_{id} \sqrt{\left(\frac{2I_{ss}}{\mu_n (C_{ox} W/2L)}\right) - (V_{id})^2} = K \frac{W}{L} V_{id} \sqrt{\left(\frac{2I_{ss}}{K(W/L)}\right) - (V_{id})^2}$$

ΔI_d for the input pair is plotted in Fig. 3.23 along with the linear approximation. The input voltage corresponding to the 1-dB compression point was calculated to be approximately

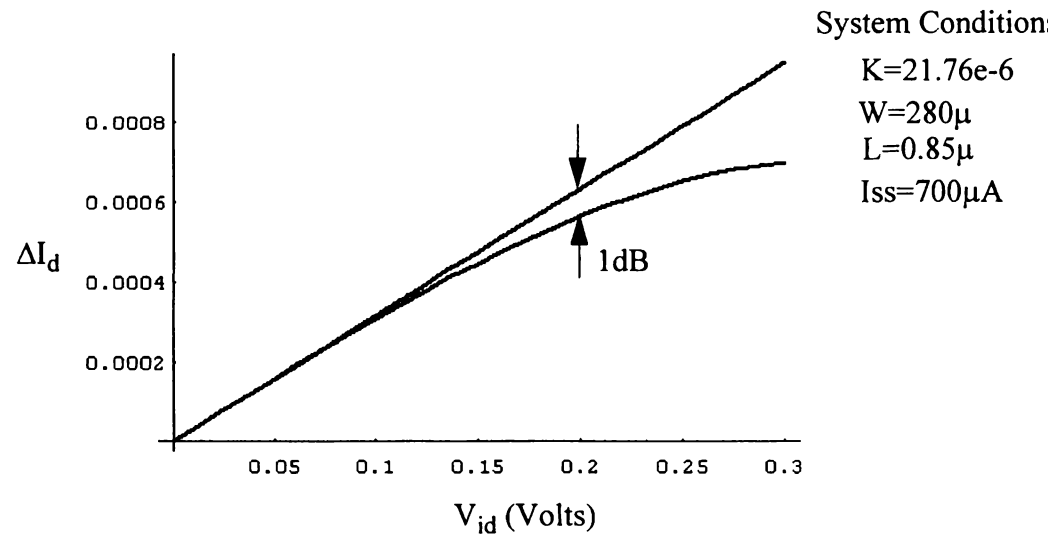


Fig.3.23 Calculated Input Pair Linearity.

200 mV which is reasonably close to the 230 mV predicted by Fig. 3.22 for IC = 19. This correspondence between the values predicted by the strong inversion equation and the simulation helps to confirm the reliability of the simulated data in strong inversion. The output stage has a common mode current level of 150 uA, thus with a 2 mS transconductance an input voltage of 150 mV will shut down one side of the output stage. Thus the maximum input range is set more by the output stage than by the input pair.

Once IC and ID are selected, the aspect ratio of the transistor is fixed and thus the only parameter left to be selected is L. Selection of L involves consideration of the trade-off between transistor matching and input capacitance/bandwidth. L was chosen to be 1.05u with more emphasis placed on minimizing input capacitance and maximizing bandwidth than on precise transistor matching.

A spread sheet based design tool developed by Dr. David M. Binkley was used to estimate the random input offset voltage resulting in a 1 sigma offset voltage of 1.9mV.

Design of the Tracking Current Sources

The tracking current sources track the tuning current of the input pair to produce a zero CM output level for the input stage, thus the CM level of the transconductor output is set by the output stage and is relatively independent of the tuning current. The design of the tracking current sources is complicated by several factors. The transconductor input CM voltage range including ground requires the current sources to have a low drop out voltage. The noise of the current sources adds directly into the signal and thus the sources must be low noise. The matching of the current sources must be reasonably good to accurately track the tuning current. And, the current levels in the current sources vary widely over the tuning range.

The low dropout voltage required to keep the input pair in the saturation region and the low noise requirement excludes the use of the cascode and the low voltage cascode current source topologies leaving the simple current source and the resistive degenerated sources as possible candidate topologies. A noise analysis comparing a the simple, long L current source shown in Fig. 3.24 A) to the resistively degenerated current source shown in Fig. 3.24 B) resulted in the following equation:

$$i_n^2 = (4kT)\left(\frac{4}{3}\right)\left(\frac{I}{V_{max}}\right)\left(\frac{(1+2\alpha)}{(1+\alpha)^2}\right) \qquad (3.1)$$

,where V_{max} is the minimum allowable output voltage of the current source and $V_{degen} = \alpha * V_{max}$. For $\alpha = 0$ the result simplifies to that of the simple current source shown in A.) where $g_m = 2\ I / V_{max}$. For $\alpha = 1$ the result simplifies to the noise of a resistor where $R = V_{max} / I$. The current source in B.) is represented by $0 < \alpha < 1$. Thus the ratio of i_n^2 for $\alpha = 1$ to i_n^2 for $\alpha = 0$ is 3/4 which is a 25% reduction in noise power. However, for a practical resistively degenerated current source α will be less than 1 resulting in a noise reduc-

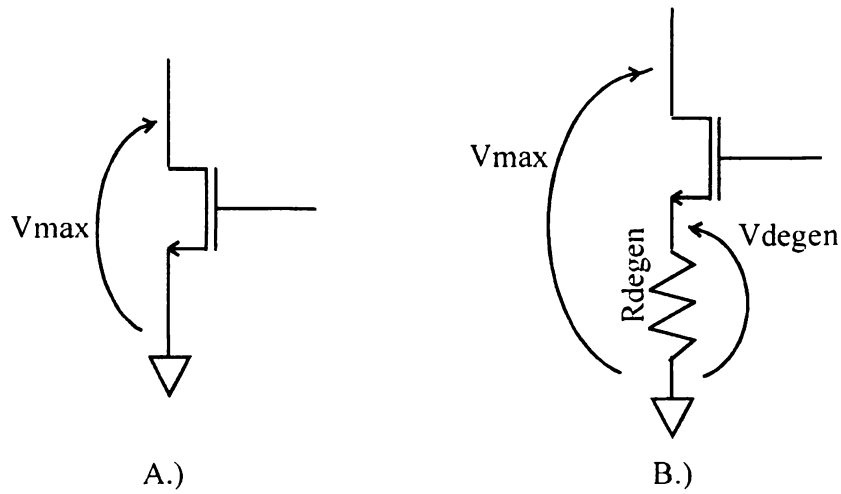


Fig.3.24 Current Source Noise Comparison.

tion in the range 15 - 20%. The degenerated sources were chosen for this noise reduction, however, it is difficult to argue that they are clearly superior to a simple long L current source, since many other issues such as matching, bandwidth, and output impedance would have to be considered. However, the degenerated sources provide adequate performance for this application which is sufficient justification for their use.

Using equation 3.1 above for

I = 350uA

Vmax = 600 mV

alpha = 2/3

the equivalent output noise current is found to be

$$i_n^2 = (4kT)\left(\frac{4}{3}\right)\left(\frac{350 \cdot 10^{-6}}{600 \cdot 10^{-3}}\right)\left(\frac{\left(1 + 2 \cdot \frac{2}{3}\right)}{\left(1 + \frac{2}{3}\right)^2}\right) = 10.84 \cdot 10^{-24}\frac{A^2}{Hz}$$

which is a factor of approximately 0.84 time the noise power of an equivalent long L current source with $\alpha = 0$, or a noise reduction of approximately 15%.

Design of the Cascode Output Stage

A similar approach was used in the design of the fixed current sources in the cascode output stage. The current in these sources is less than half the nominal current in the tracking current sources thus from the equation in the previous section, the noise contribution of the fixed current sources is approximately half that of the tracking sources for the same values of V_{max} and α. The theoretical noise value is calculated below for $\alpha = 0.72$, V_{max}=500 mV, and I = 150 uA, yielding

$$i_n^2 = (4kT)\left(\frac{4}{3}\right)\left(\frac{150 \cdot 10^{-6}}{500 \cdot 10^{-3}}\right)\left(\frac{(1+2 \cdot 0.72)}{(1+0.72)^2}\right) = 5.47 \cdot 10^{-24}$$

The voltage at the gates of the cascode transistors is set by the gate to source voltages of transistors M12, M13 and increases as the tuning current increases. This bias approach was chosen to allow more head room for the tracking sources for larger values of tuning current. Further investigation suggests that this approach is not optimum because for higher current levels the input pair approaches the ohmic region. At higher tuning currents the drain voltage for the input devices should actually decrease slightly to compensate for the smaller threshold voltage produced by the body effect. Thus, for the production version, the voltage at the sources of the cascode devices should be fixed or possibly even decrease for higher tuning currents.

Transconductor Noise Analysis

The noise contribution of the input pair is to first order

$$i_n^2 = 2 \cdot \left(4kT \cdot \frac{2}{3} \cdot g_m\right) = \frac{16}{3} kT \cdot 2mS = 44.26 \cdot 10^{-24} \frac{A^2}{Hz}$$

which agrees well with the simulated value of $46.5*10^{-24}A^2/Hz$. Table 3.6 below summarizes the calculated and simulated output noise current for each of the significant noise contributors in the transconductor.

3.4 Tuning Circuit

The tuning block schematic is shown in Fig. 3.25 and consists of the master transconductor shown in Fig. 3.20, a tuning current control cell shown in Fig. 3.26, and a bias cell shown in Fig. 3.27. The bias cell provides the output common mode current for the transconductors and two 100uA currents for tuning purposes. To tune the transconductance to the on-chip resistor, node 3 is connected to node 15 and node 4 is connected to ground. One of the 100uA currents flows through the resistor composed of the parallel

Table 3.6: Calculated and Simulated Transconductor Noise Contributions

Noise Source	Calculated Noise Current (A^2/Hz)	Simulated Noise Current (A^2/Hz)
Input Pair	$44.16*10^{-24}$ A^2/Hz	$46.5*10^{-24}$ A^2/Hz
Tracking Current Sources	$21.7*10^{-24}$ A^2/Hz	$22.0*10^{-24}$ A^2/Hz
Fixed Current Sources	$10.96*10^{-24}$ A^2/Hz	$10.8*10^{-24}$ A^2/Hz
Total	$76.82*10^{-24}$ A^2/Hz	$79.3*10^{-24}$ A^2/Hz
Input Referred Noise Voltage	4.38 nV/rt-Hz	4.45 nV/rt-Hz

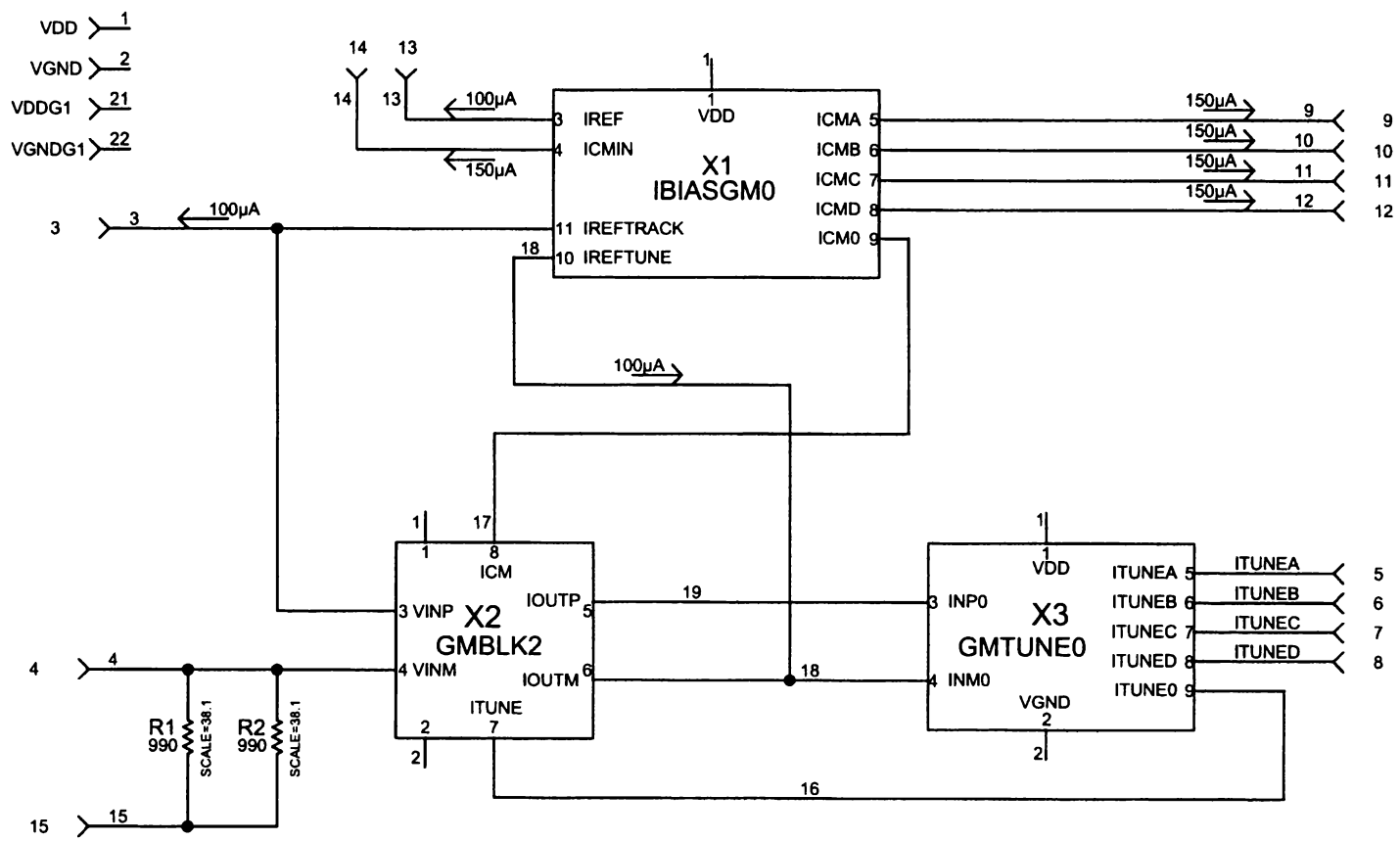


Fig.3.25 Tune Block Schematic.

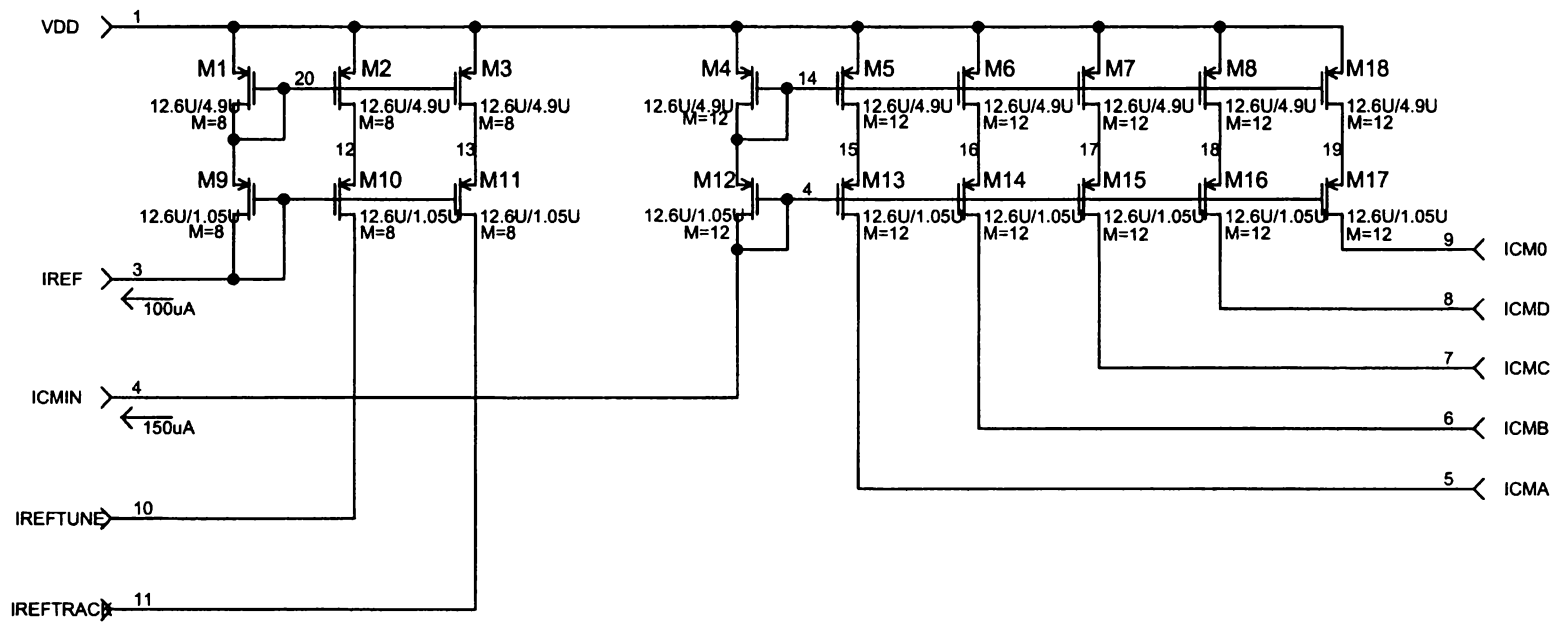


Fig.3.26 IBIASGM0 Schematic.

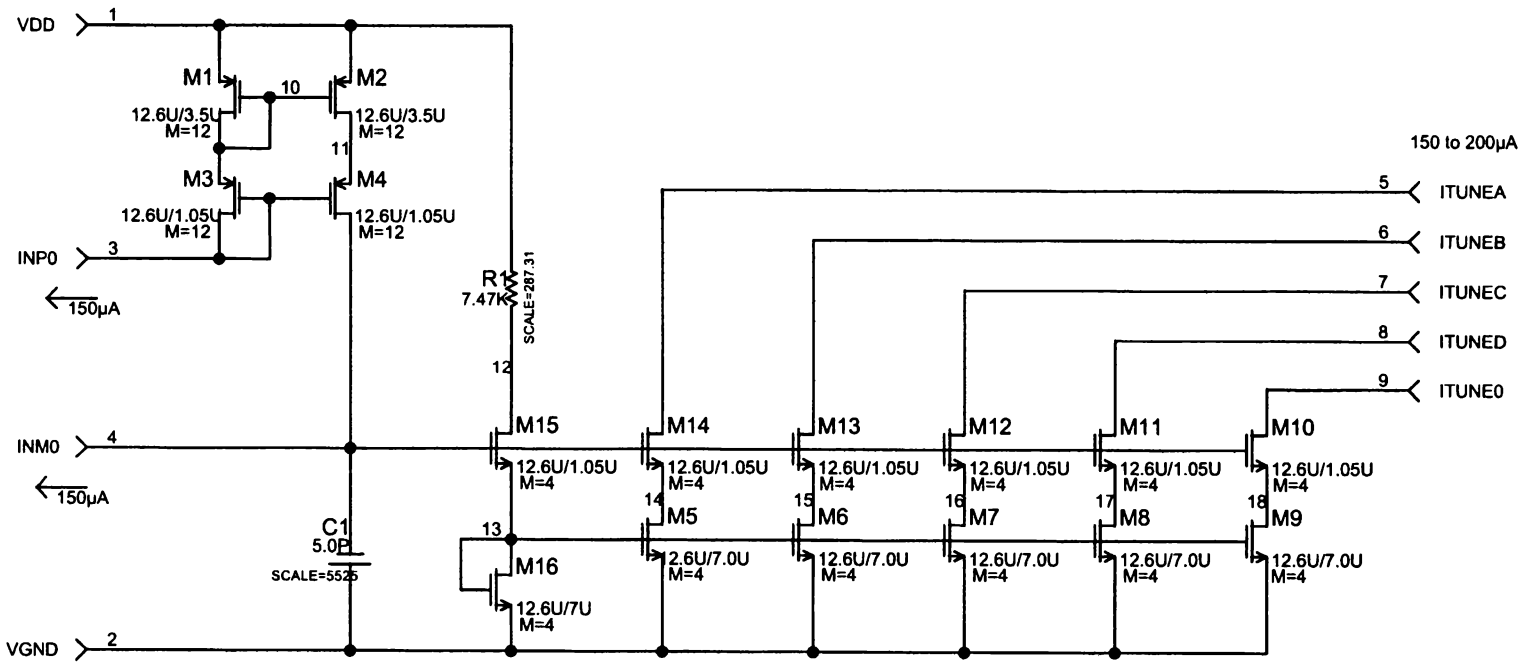


Fig.3.27 GMTUNE0 Schematic.

combination of R1 and R2 producing a 50mV voltage between the transconductor inputs. The second 100uA current is used to create an output offset current of 100uA. The tuning current control cell subtracts Ioutp from (Ioutm + 100uA) and adjusts the transconductor bias current (Itune) until the error current is zero. When this occurs, the differential output of the transconductor is 100uA and the transconductance is 100uA/50mV = 2mS. Variation in the tuning resistance and random transconductor input offsets change the effective voltage across the transconductor inputs and thus affect the resulting transconductance.

Startup/Tuning Range

The startup characteristics of the tuning loop were studied by breaking the loop at the output of gmtune0, node 16 in Fig. 3.25, and sweeping the master transconductor bias current. The tuning current at the output of gmtune0 was then plotted for several different values of Rtune, over the transistor corner models, and for 25 and 60 degrees C. The resulting plots for the worst case corner (fast N, slow P) are shown for 25 and 60 degrees C and for tuning resistance values ranging from 400 ohms to 475 ohms in steps of 5 ohms are shown in Fig. 3.28. The possible operating points for each curve are the intersection of the curve with the line y = x. The first intersection point is the desired stable operating point. The second intersection point, if it exists, is unstable. The bias current of the circuit converges to the stable operating point for current values to the left of the unstable intersection, but diverges to the maximum allowed current for values to the right of the unstable intersection. This unstable operating point results in a tuning loop that will operate correctly if started in the stable region of operation, but will latch up if started in the unstable region. For the cases where the curve never intersects the line y = x, no stable point exists and the

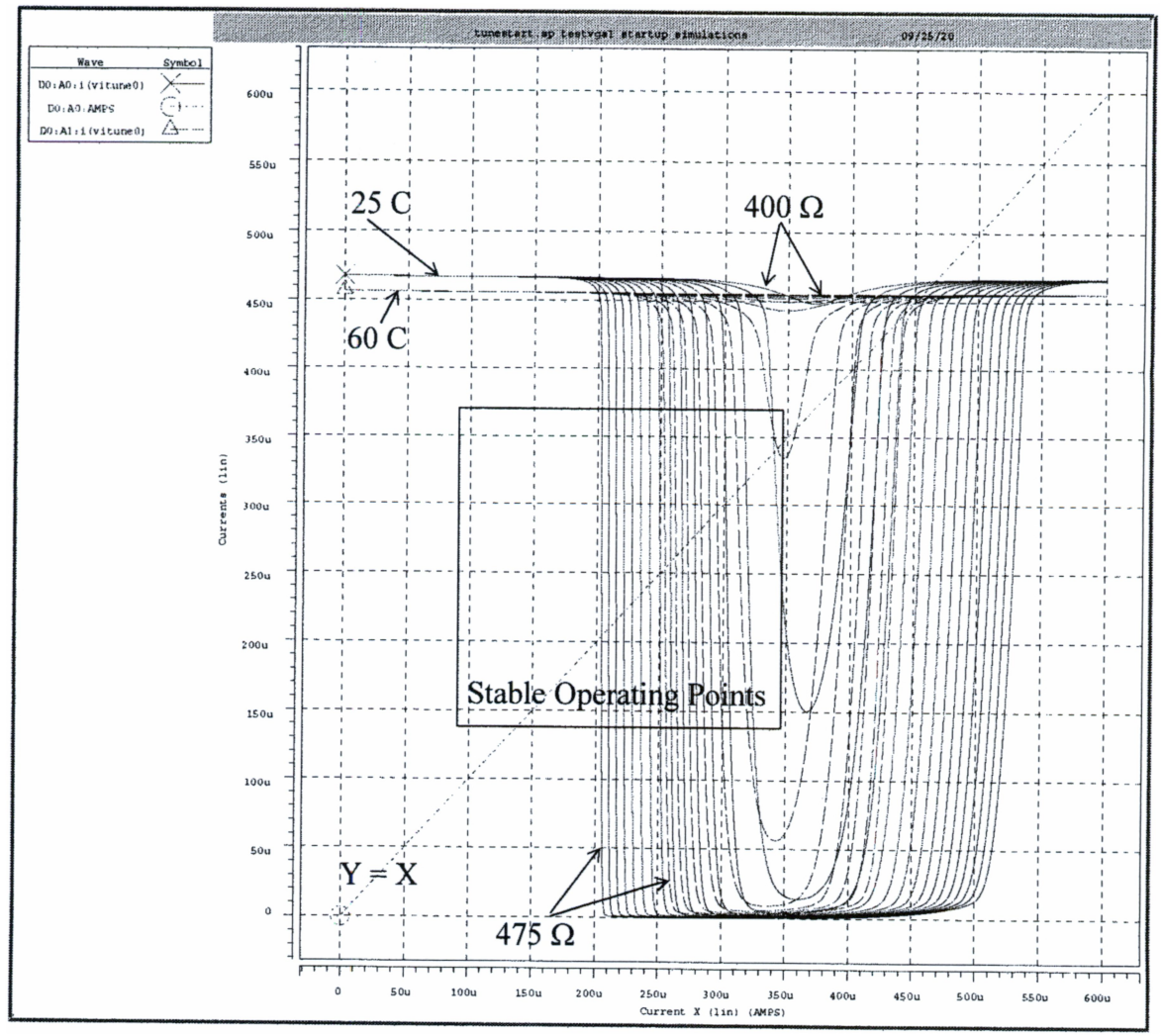


Fig.3.28 Worst Case Tuning Loop Startup Simulation.

current diverges to the maximum allowed current regardless of the startup conditions. For the worst case corner model used to generate Fig. 3.28, the tuning loop would not lock for the 20% low polysilicon case (R_{tune} = 400 Ω) and would have unstable regions of operation for resistors that are only 10% low. While this corner is extreme and would seldom be seen in production a robust design should operate over all of the corner models to provide good yield in production, also other factors such as random transconductor input offset produce similar results by reducing the effective tuning voltage, thus the tuning scheme could fail even for typical device characteristics. Clearly this problem must be corrected for the production version of the chip.

A start-up circuit could be used to force the tuning loop into the correct region of operation. However, this would not solve the problem for the curves with no stable operating point and also could be complicated to implement. A better approach is to modify the transconductor so that the second intersection occurs at a larger tuning current and then limit the maximum tuning current so that the second intersection can never occur. Simulation of the transconductor shows that the turn up in the curves is the result of a non-monotonic relationship between the transconductance of the transconductor and the bias current. Starting at low bias currents, the transconductance of the input differential pair increases and the drain to source voltage (Vds) of the input pair decreases for increasing bias currents. Finally, Vds becomes small enough that the input pair begins to approach the ohmic region and the transconductance of the input pair begins to decrease as the bias current increases. The bias current at which this occurs can be moved higher by increasing the W/L ratio of the input devices and/or by lowering the drain voltages of the input pair to change the point at which the input devices begin to enter the ohmic region. Increasing the

W/L ratio of the input devices lowers Vdsat for the devices and improves the matching, thus reducing the random offsets, but also reduces the linearity of the input pair and increases the input capacitance. Lowering the drain voltages of the input pair provides more headroom for the input devices but reduces the available voltage for the tracking current sources which degrades the current source noise performance. Due to the need for significant improvement in this area of performance, both of the proposed modifications may have to be used, while paying careful attention to the trade-off between linearity and noise.

3.5 Conclusions

The design of the various components of the VGA was presented in this chapter. The design of the attenuator was discussed first. The final attenuator design consists of two series tapped resistor attenuators with a nominal input resistance of 1 kΩ. The simulated bandwidth and delay dispersion are 311 MHz and 380 ps respectively. Next, the design of the tuned transconductor was discussed. The final transconductor design consists of a tuned differential pair input stage with a folded cascode output stage. The transconductor has a simulated bandwidth of 150 MHz and a simulated input equivalent noise voltage of 6.8 nV/rt-Hz. The calculated 1dB compression point for the input pair is 200 mV, but the linear input range is limited to 150 mV by the output stage. The calculated 1 sigma input offset voltage is 1.9 mV. The transconductors are arranged in a master-slave configuration in which the signal transconductors are slaved to a static master transconductor embedded in a feedback loop. The feedback is used to establish the desired transconductance in the master transconductor by adjusting the bias current. This bias current is then mirrored to

the slave signal transconductors. A flaw was discovered in the start-up of the tuning loop which must be corrected for the production version and a possible solution was discussed.

Chapter 4 Experimental Results

4.1 Prototype 1

4.1.1 Objectives

The primary objectives of the Prototype 1 chip were to evaluate the two series attenuator structures discussed in section 3.2, the transconductor, and the transconductor tuning scheme. The bandwidth and gain accuracy of the attenuators and the gain, bandwidth, and offset of the transconductors were of primary concern. However, the tuning scheme and matching of the slave bias currents (I_{tune}) were also investigated.

4.1.2 Circuit Description

The top-level block diagram for prototype 1 is shown in Fig. 4.1. The chip contains four VGA channels which include a differential output channel and a single ended output channel for the series/parallel attenuator and for the large version of the continuos polysilicon attenuator discussed in Chapter 3. The differential outputs allow measurement of the common mode currents and provide the highest bandwidth of the two output types for high-frequency tests such as risetime measurements. The single-ended outputs reduce the bandwidth slightly, but facilitate single-ended measurements such as gain and noise measurements. Additional circuits on the chip include an attenuator of each type, various test resistors, and the tuning circuit. Each of the four slave tuning currents produced by the tuning circuit were connected to output pads to allow evaluation of the current mirror matching.

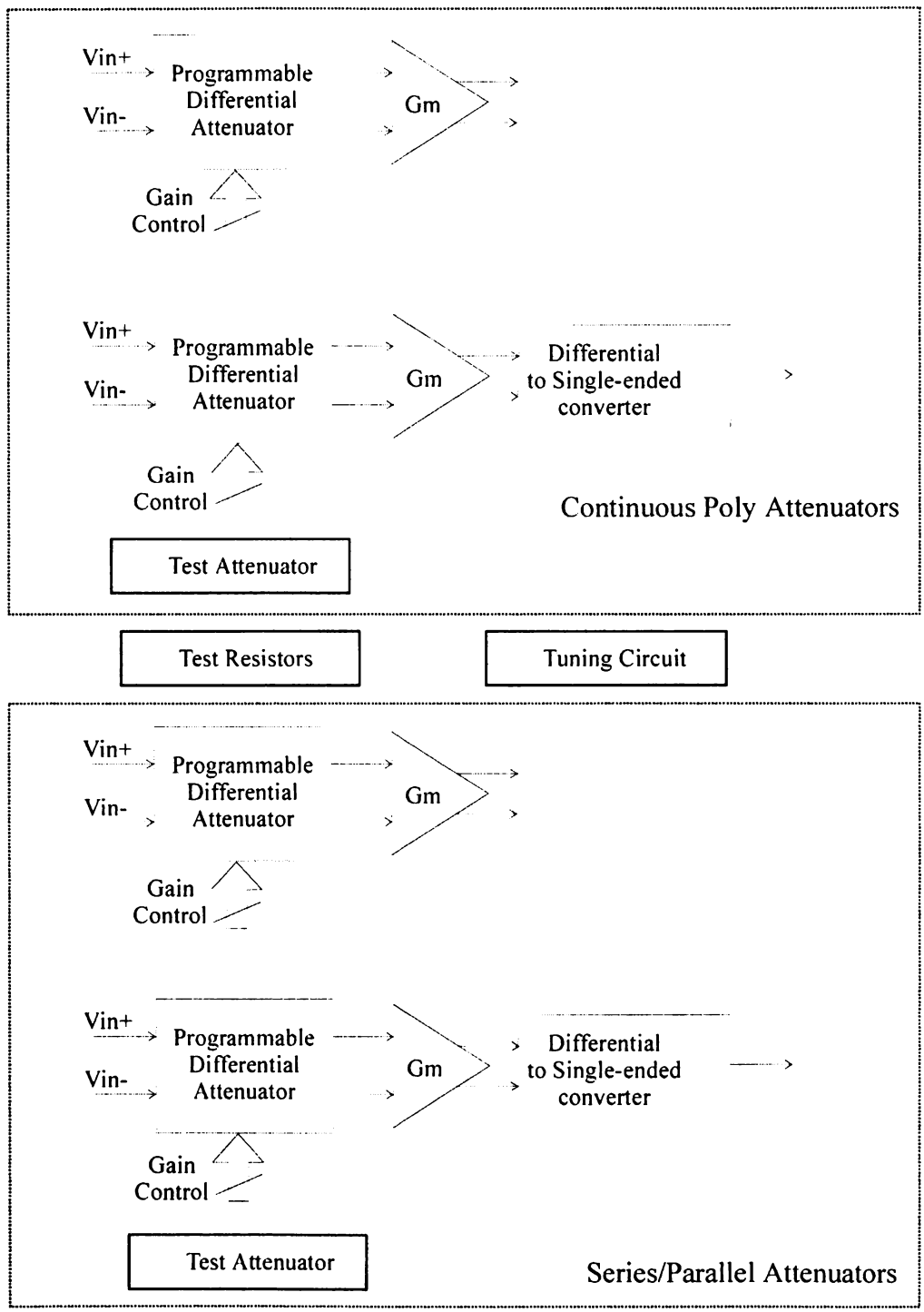


Fig.4.1 Prototype 1 Top-Level Block Diagram.

4.1.3 Layout

The Magic layout for prototype 1 is shown in Fig. 4.2. The circuits based on the continuous polysilicon attenuator occupy the upper portion of the layout and the circuits based on the series/parallel attenuator occupy the lower portion of the layout. The master and slave transconductors are identified in the figure along with one of each to the two types of attenuators. The dimensions of the layout are approximately 2.2 mm x 2.2 mm resulting in an area of 4.84 mm^2.

4.1.4 DC Measurements

Fig. 4.3 shows the DC test board for prototype 1. The socket for the prototype chip is a through-hole component, thus, the board is constructed with the socket on the bottom side

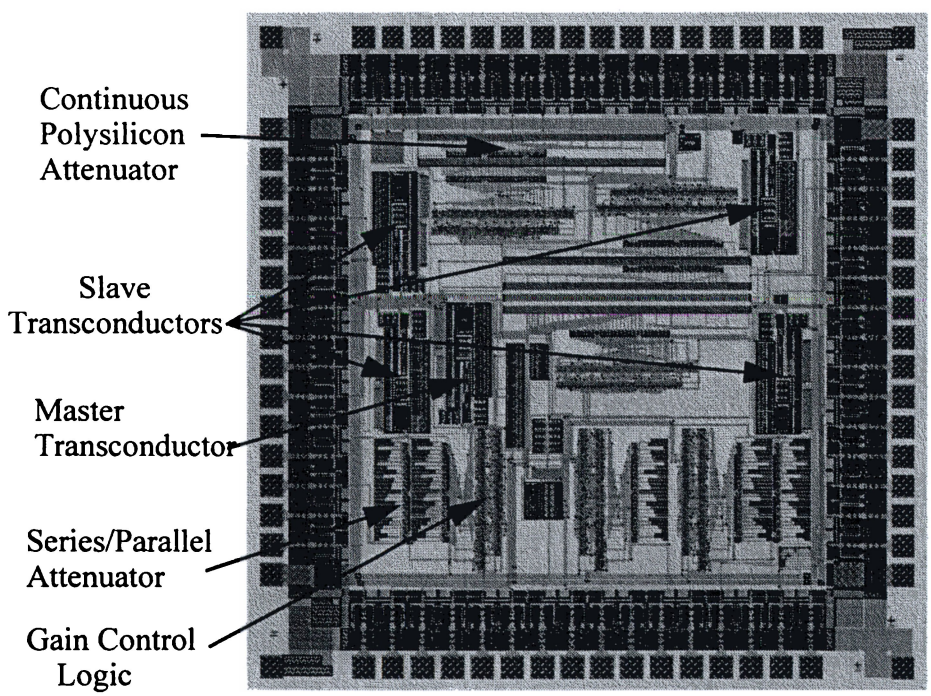


Fig.4.2 Prototype 1 Magic Layout.

of the board to allow short-lead-length connections to the supporting circuitry and the ground plane. The DC board was used for the offset, gain setting, and current mirror matching measurements.

Offset

The transconductor offsets were measured by grounding both inputs to the transconductor of interest and measuring the differential output voltages (*Voutoff*) for the maximum gain setting with the transconductor loaded with off-chip 500Ω loads. Next, a 50mV input signal was applied and the output voltage (*Vout*50) was measured. Since $Voutoff = AVos$ and $Vout50 = A(Vos + 50mV)$, the channel gain (A) can be eliminated by forming the ratio

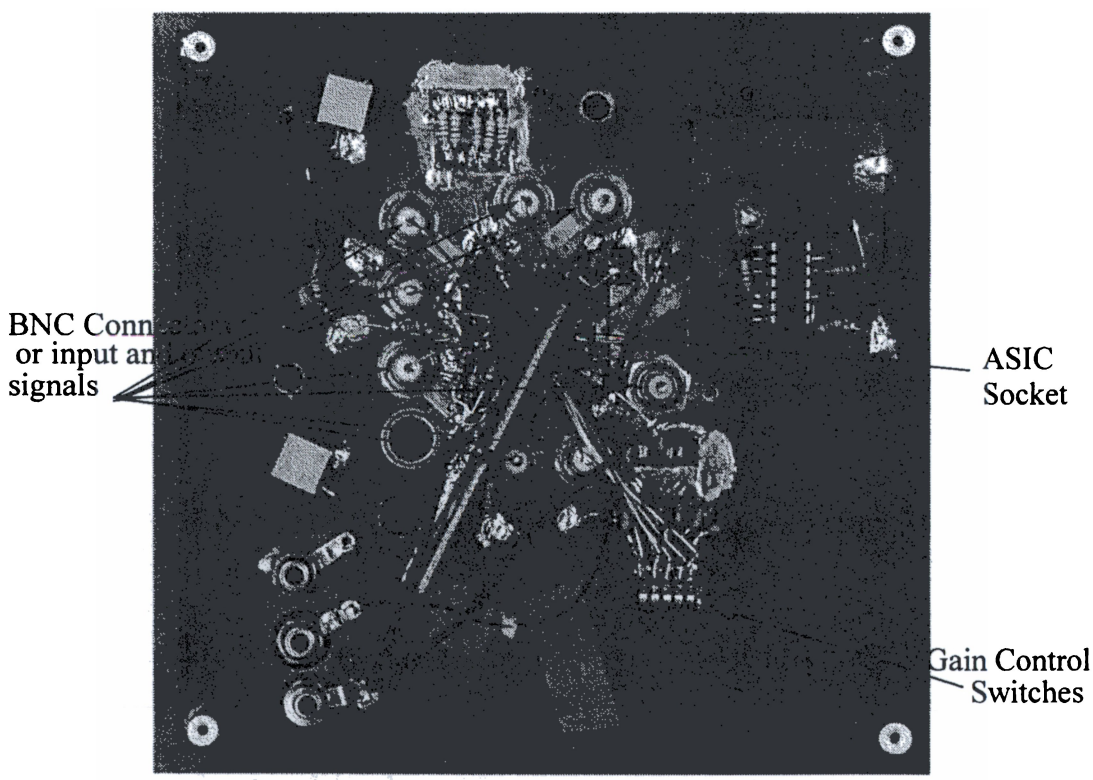


Fig.4.3 Prototype 1 DC Test Board.

$$K = (Vout50)/(Voutoff) = \frac{Vos + Vin}{Vos} .$$

Thus, the input referred offset voltage can be calculated from the two measured output voltages using

$$Vos = \frac{Vin}{K-1} = \frac{50mV}{K-1}.$$

The resulting input referred offset voltages are reported in Table 4.1.

The measured input offset voltages were used to calculate the summary statistics and to plot the associated Gaussian distribution shown in Fig. 4.4. The mean of 0.032 mV is very consistent with the expected zero mean. The Gaussian distribution is an estimate of the probability distribution function of the offset voltage and indicates a 3 sigma value of approximately 5mV. Because the slave transconductor are exact duplicates of the master transconductor, this 5mV value should also apply to the master transconductor and thus the effective tuning voltage seen by the master transconductor has a 3 sigma variation of approximately 10%, which translates directly into a 3 sigma gain error of 10% in the slave transconductors. This value is larger than is desirable, however, improvement in the offset characteristics of the transconductor would require the use of larger input devices which would degrade the bandwidth performance. Additionally, these gain errors caused by the offset voltage of the master transconductor affect all of the slave transconductors on a given chip in the same way. Thus, the gain matching from channel to channel on the chip is not affected and the resulting gain errors do not result in degraded position information from the block detector attached to the chip.

Table 4.1: Measured Input Referred Offset Voltages for Prototype 1

Chip #	Channel 1 (mV)	Channel 2 (mV)	Channel 3 (mV)	Channel 4 (mV)
1	-1.41	-1.06	-0.70	4.02
2	-1.92	-0.05	1.00	-0.82
3	2.05	3.59	1.63	-2.32
4	-0.64	-0.14	0.99	-1.56
5	1.31	-0.36	4.56	2.90
6	0.27	-1.04	-0.61	1.13
7	0.29	-0.38	-0.72	-0.13
8	2.39	0.70	0.34	-0.72
9	-1.03	0.57	0.68	0.03
10	0.87	-1.02	0.06	-3.43
11	-1.48	-1.24	0.89	1.32
12	-0.98	1.00	0.11	1.14
13	-2.36	-0.15	0.19	0.56
14	0.43	-0.59	-0.88	0.70
15	3.36	0.93	3.19	-1.09
16	0.48	0.33	-0.74	1.73
17	2.25	-0.86	0.80	-1.45
18	5.12	-0.05	-0.46	-2.77
19	-0.74	-0.81	0.69	1.64
20	-1.52	-3.35	1.74	-0.81
21	-0.96	-2.34	-1.12	-2.67
22	-0.23	-0.97	-0.06	-0.84
23	-0.37	-1.96	0.28	0.48
24	1.38	-2.66	1.34	1.64
25	-3.12	-1.48	1.56	-0.27

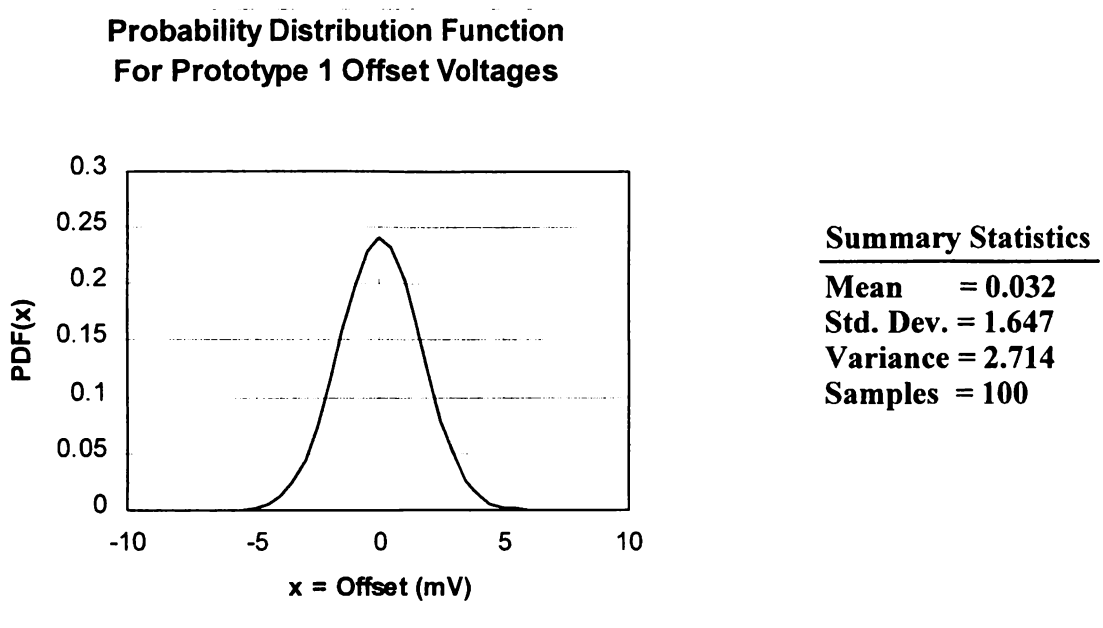


Fig.4.4 Gaussian Distribution of Measured Input Referred Offset Voltages.

Gain Settings

The gain settings for the continuous polysilicon attenuator based VGA were measured by applying a 50mV dc voltage at the input of the VGA and measuring the differential output voltage across the 50Ω loaded outputs for each of the gain settings. Fig. 4.5 shows the raw gain data. The raw data was then offset corrected by subtracting the measured output offset voltage from the measured output voltage for each channel. The resulting gains are plotted in Fig. 4.6 on a linear scale and in Fig. 4.7 on a log scale to show the linear in dB nature of the gain steps. The gains are approximately 8% lower than was initially expected as can be observed in Fig. 4.6. For example, the maximum gain setting with a gain code of 25 was expected to have a gain of 0.1v/v but has an average measured gain of 0.092v/v. The cause of the reduced gain was determined to be non-negligible resistance in

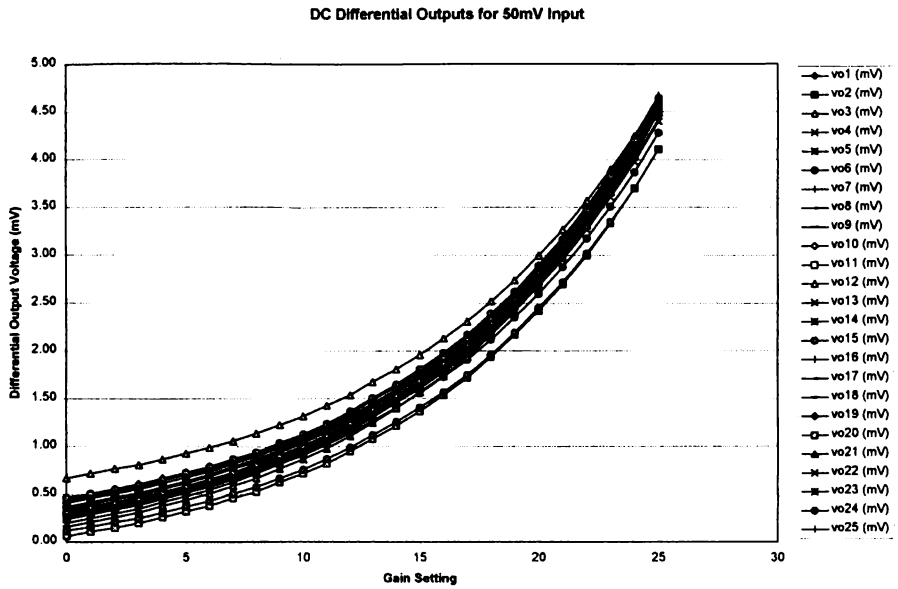


Fig.4.5 Output Voltage vs. Gain Code for a 50 mV Input- Raw Data.

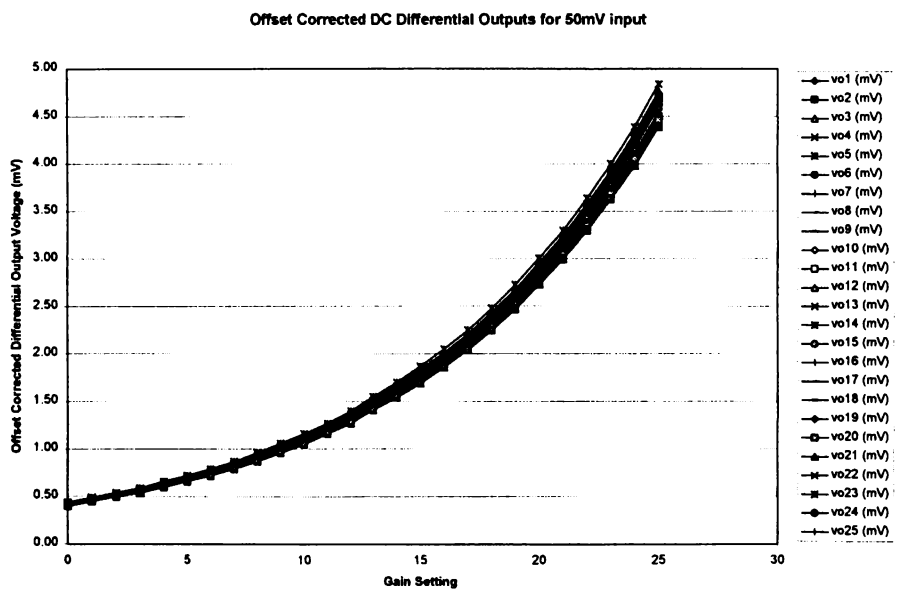


Fig.4.6 Output Voltage vs. Gain Code for a 50 mV Input - Offset Corrected.

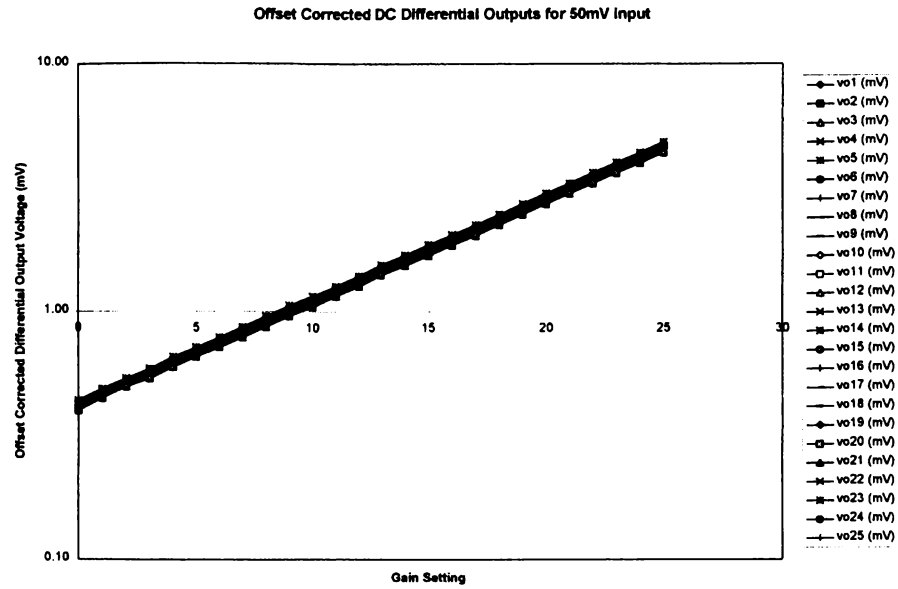


Fig.4.7 Output Voltage vs. Gain Code for a 50 mV Input- Offset Corrected, Log Scale.

the input traces and in the connections to the tuning resistor. The input traces were found to add as much as 40Ω of resistance in series with the inputs resulting in an approximate 4% loss at the input of the attenuator due to voltage division. The resistance in the trace connecting the 500Ω tuning resistor to the master transconductor was approximately 15Ω resulting in an effective tuning resistance of 515Ω which produces another ~3% gain loss. These two effects combined account for the majority of the observed gain discrepancy.

Current Mirror Matching

The tuning current for all four channels of each chip was measured using a Keithly 2000 multi meter connected between vdd and the tuning current outputs. The measured currents are listed in Table 4.2. The measured values for each channel were normalized to the mean value for the chip containing that channel. These normalized values were then

Table 4.2: Tuning Current Matching Data

Chip #	Itune A (uA)	Itune B (uA)	Itune C (uA)	Itune D (uA)	Chip Average (uA)
6	131.26	132.05	131.88	132.09	131.82
8	144.82	144.95	144.75	144.88	144.85
9	138.14	138.21	137.87	137.97	138.05
10	147.83	148.74	148.35	149.23	148.50
11	148.77	148.59	149.29	149.35	149.00
12	135.73	135.88	136.05	136.34	136.00
13	146.28	146.55	146.70	146.96	146.62
14	144.56	144.90	144.94	145.49	144.97
15	138.00	138.30	138.12	138.70	138.28
16	146.95	147.28	147.34	147.86	147.36

used to calculate the percent error for each channel relative to the chip mean. The percent error values were used to calculate the summary statistics and to generate the Gaussian distribution shown in Fig. 4.8. The percent gain error due to the matching of the tuning currents is insignificant compared to the error due to the offset in the master transconductor and thus the tuning current mirror matching is more than adequate.

4.1.5 AC Measurements

Fig. 4.9 shows the AC test board for prototype 1. The AC board is also constructed with the socket on the bottom side of the board to allow tight connections to the supporting circuitry and the ground plane. Due to the high frequencies of the input and output signals, the signal connections are made using RG174 coaxial cable with the shielding soldered directly to the ground plane. This construction technique provides a 50Ω signal

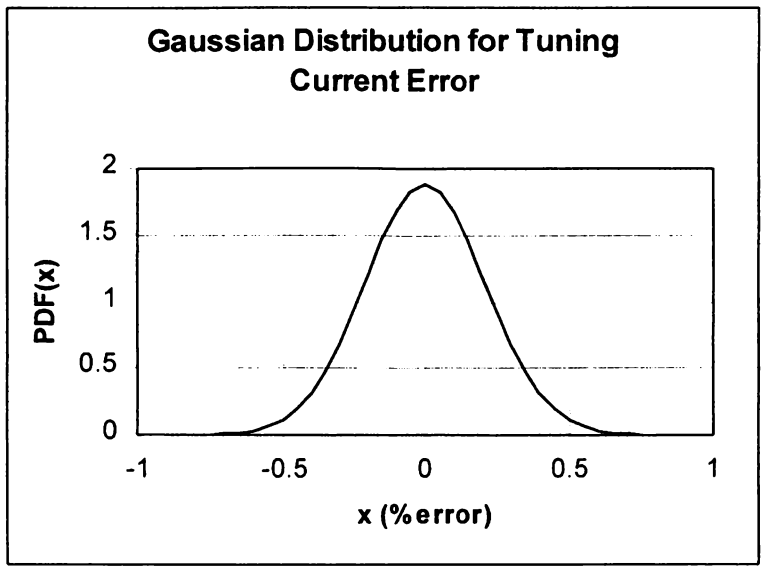


Fig.4.8 Gaussian Distribution of Percent Matching Error for Itune.

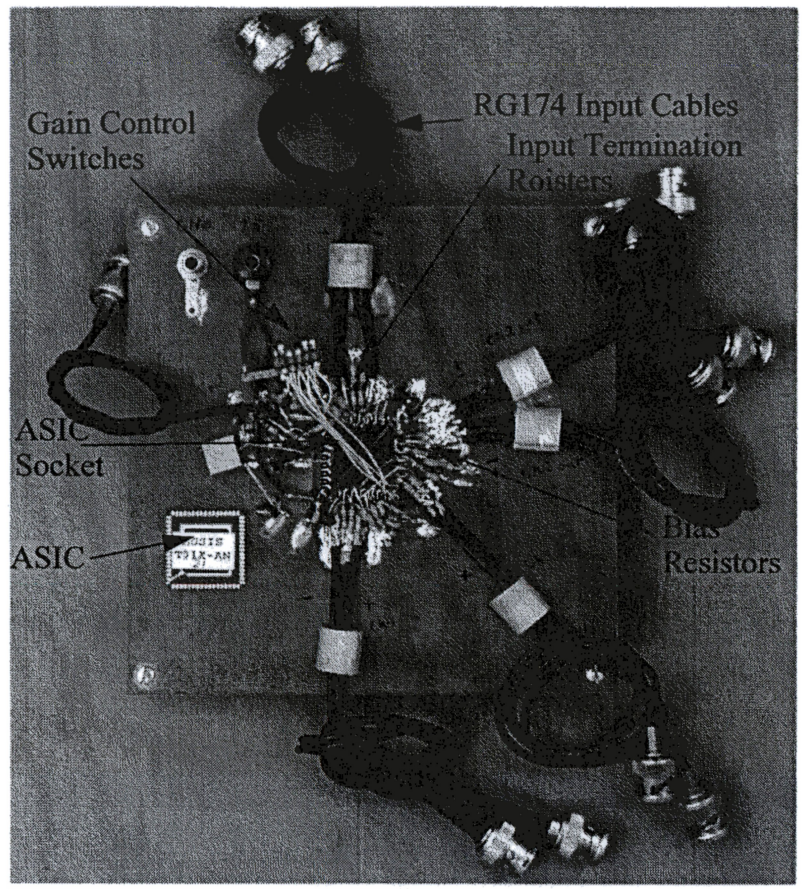


Fig.4.9 Prototype 1 AC Test Board.

path all the way up to the socket. The AC board was used for the risetime, delay dispersion, and crosstalk measurements.

Bandwidth/Risetime

An HP3589A network analyzer was used to measure the transfer function of the VGA. The measurement was made on the single-ended version of the continuous polysilicon attenuator based VGA. The network analyzer has a maximum frequency of 150MHz which is approximately equal to the expected bandwidth of the VGA. However, the measured spectrum shown in Fig. 4.10 appears to exhibit some peaking near 120MHz and indicates a higher than expected bandwidth. Further analysis was performed in the time domain using a 1ns rise-time HP 8082A pulse generator and a 350MHz Tektronix 2465A oscilloscope to observe the risetime and overshoot of the differential output of the tapped resistor attenuator based circuit in response to a 1ns risetime input pulse. Fig. 4.11 shows a

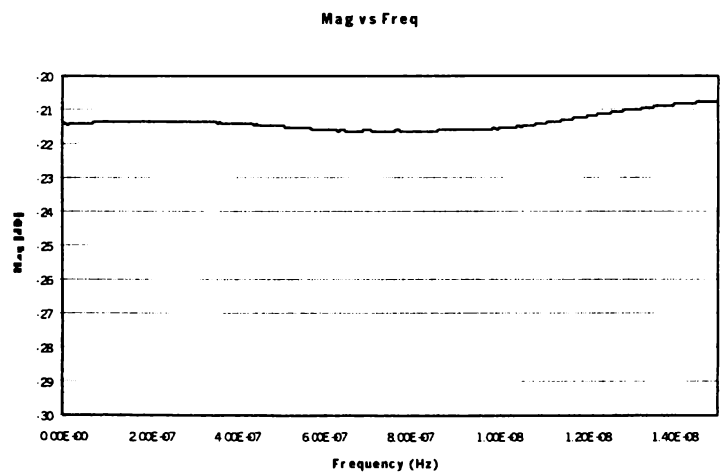


Fig.4.10 Prototype 1 Magnitude Plot of the Transfer Function.

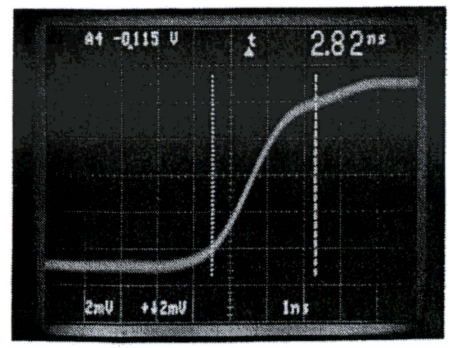


Fig.4.11 Pulse Response for Prototype 1 with Maximum Gain Setting.

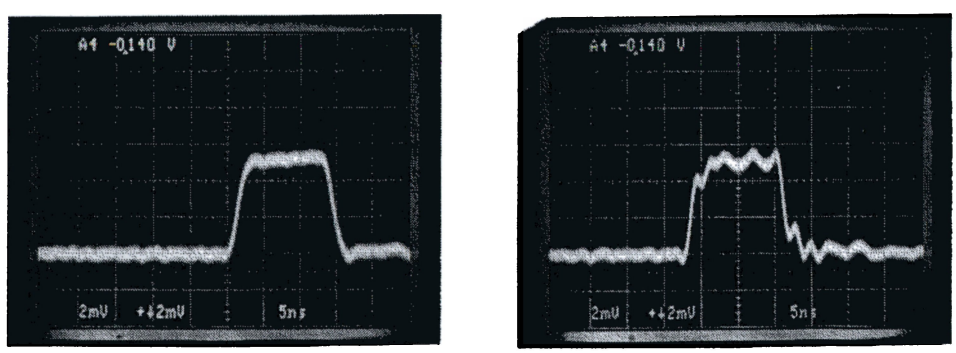
typical pulse response for the maximum gain setting for a 1 ns risetime input pulse with amplitudes of 50 mv. Correcting the 2.8 ns risetime to remove the risetime of the pulser and the scope results in a risetime of 2.4 ns or a bandwidth of approximately 145 MHz, which is closer to the expected value. The signal also appears to be distorted which makes the risetime appear longer than it otherwise would be, suggesting the higher bandwidth indicated by the spectrum analyzer is probably more accurate.

Delay Dispersion

The delay dispersion over the gain range was measured for the differential output, continuous polysilicon attenuator based VGA using a Techtronix 2465A oscilloscope and an HP 8082A pulser. The delay was measured by choosing the maximum gain setting as the reference delay and observing the time shift of the signal mid-point as the gain was adjusted over the full scale. The measured delay shift increased to a maximum value of 750ps at the gain code of 17 and then decreased to 150ps as the gain was reduced further resulting in a maximum delay dispersion of 750ps, which is consistent with the post-layout simulation.

Feedthrough

While observing the AC response for the differential output of the continuous polysilicon attenuator based VGA, some feed through was observed. Fig. 4.12 a.) shows the response of the VGA to a 50 mV input signal and maximum gain, and b.) shows the response of the VGA to a 500 mV input signal and minimum gain. The minimum gain response exhibits a large amount of feed through which could explain the apparent peaking observed using the network analyzer. The feed through is most pronounced for minimum gain due to the larger input signal associated with this gain setting. The feed through path could not be determined for the Prototype 1 chip. The most likely locations for the feed through path are the socket, package, and bondwires of the prototype chip and board and the on-chip bias rings for the ESD protection diodes. One of the issues that hindered analysis of this effect is the limited wideband gain that can be obtained from the current mode outputs. The output pads, package pins, and testboard socket add 10 - 20 pF of parasitic capacitance to the outputs which requires that the effective resistance at the outputs to



a.) b.)

Fig.4.12 Pulse Response Photographs Showing Feedthrough for Prototype 1 for a.) Maximum Gain and b.) Minimum Gain.

be very low to maintain a high bandwidth. However, because the output resistance performs the current to voltage conversion for the signal, the small load resistance results in a low gain.

The above feed through results indicate significant coupling between pins and/or pads on the prototype. Because the production chip will be a mixed mode design, the crosstalk between a "logic" signal input and the output of the VGA was investigated. Fig. 4.13 shows a 3.3 volt "logic" signal applied to at test resistor located several pins away from the VGA input and the resulting single-ended VGA output for maximum gain. The response shows a significant amount of crosstalk indicating a need for further isolation.

4.1.6 Prototype 1 Conclusions

The data from prototype 1 shows that the continuous polysilicon attenuator based VGA has sufficient bandwidth and gain accuracy to meet the requirements of the Phase II ASIC. The bandwidth of the attenuator and transconductor combined is in excess of 140 MHz which is well above the required 100 MHz required for the system. The gain settings are monotonic and predictable, and the tuning scheme appears to be effective and stable. The primary areas of concern are the feed through and crosstalk observed in the time domain pulse response measurements. A second protoype was designed and fabricated to allow further study of the feed through and crosstalk issues.

4.2 Prototype 2

4.2.1 Objectives

The primary objectives of the Prototype 2 chip were to improve the feed through characteristics of the Prototype 1 chip and to investigate the matching and crosstalk between a

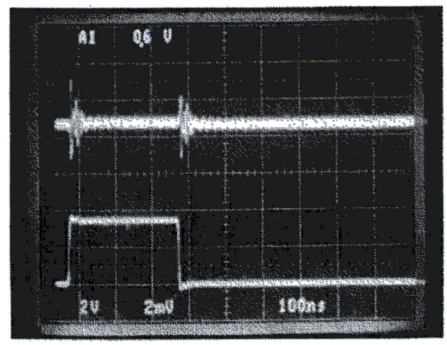


Fig.4.13 Response of Prototype 1 50ohm output due to crosstalk due to a 3.3 v "logic" input signal.

four-channel system of VGAs. Additionally, buffered outputs were added to allow better noise and crosstalk measurements than were possible with Prototype 1, the attenuator was-modified to reduce the attenuator layout area, and an input test pulse generator was added.

4.2.2 Circuit Description

The top level schematic for Prototype 2 is shown in Fig. 4.14. The prototype includes all four channels needed for the final Phase II ASIC design. A schematic of the channels is shown in Fig. 4.15. Each channel includes a modified version of the attenuator, a transconductor, a two-output current mirror that provides two pairs of differential current outputs, and a test pulse generator.

The size of the attenuator structures was reduced by a factor of two in both dimensions, which reduces the required area by a factor of four and increases the bandwidth. All unused taps of the attenuator were removed to reduce the length of the attenuator. Fig. 4.16 shows the new attenuator and the old attenuator on the same scale.

As shown in Fig. 4.15, two differential outputs are supplied by the VGA channel. 5kΩ loads are used to convert the current signals from the two outputs to voltage signals. One

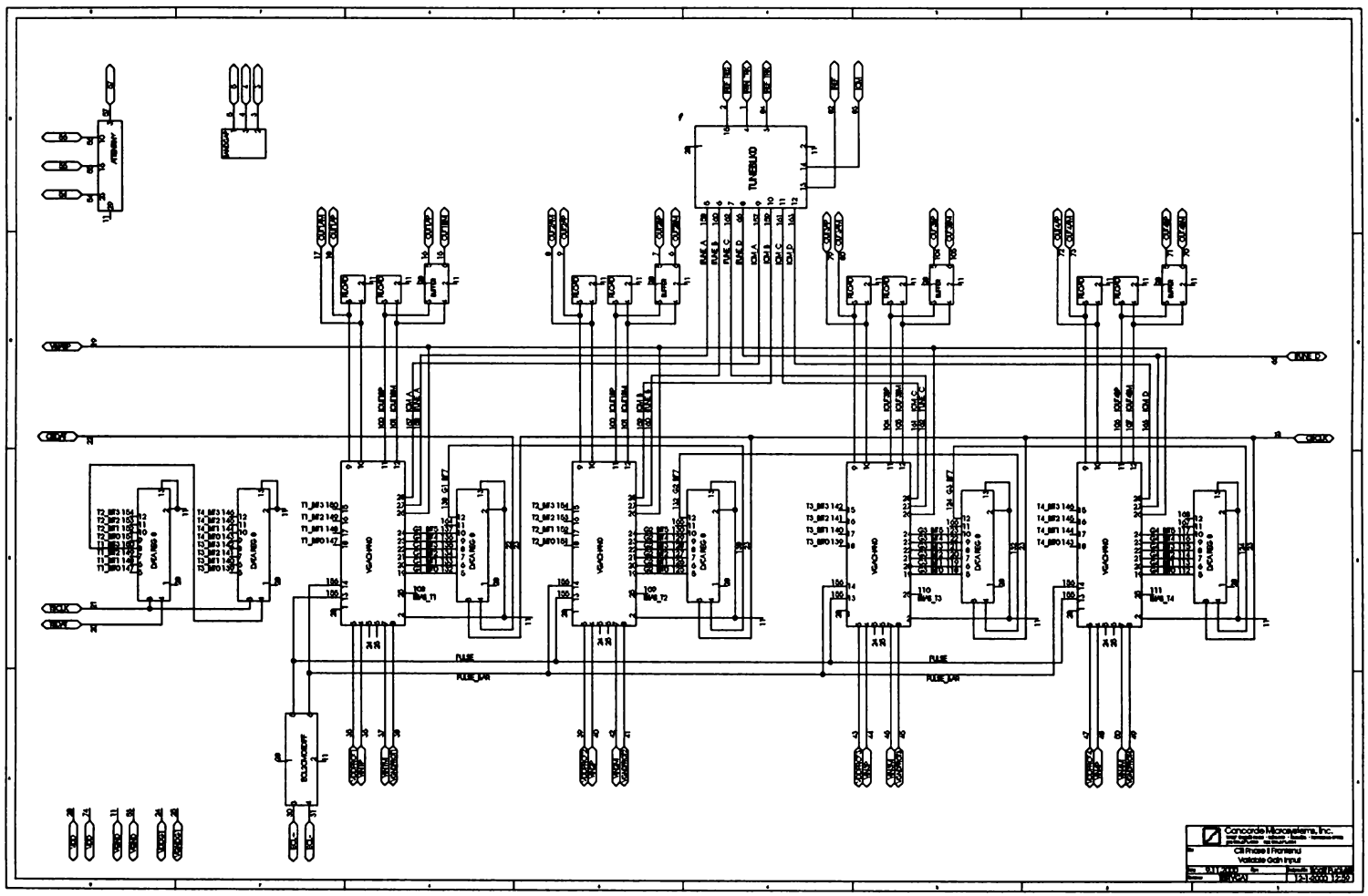


Fig.4.14 .Prototype 2 Top Level Schematic.

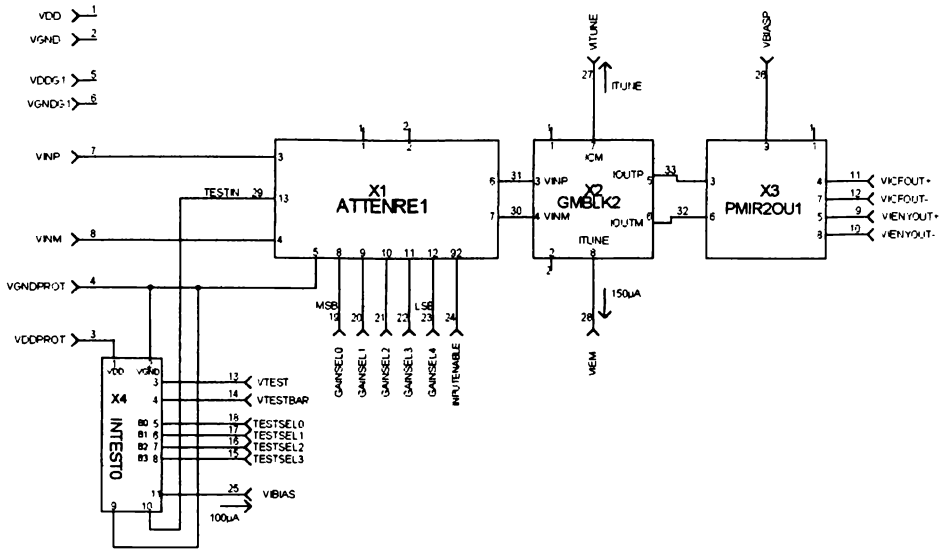


Fig.4.15 VGA Channel Schematic.

Fig.4.16 Prototype 1 and Prototype 2 Attenuators on the Same Scale.

output is then connected directly to output pads and can be used for dc gain measurements and for low gain AC measurements. The second output is buffered using source followers before going to output pads in order to provide a higher gain AC output at the expense of gain accuracy. The high gain outputs provide better immunity to noise that is injected at the outputs, and thus are valuable for crosstalk measurements. Additionally, they provide outputs with sufficient gain and bandwidth for noise measurements and other frequency domain measurements using the HP 3589A spectrum analyzer.

The input test circuit (intest0 in Fig. 4.15) allows on-chip generation of analog test pulses. The pulses allow testing of the channels with no external analog signal present. The channel is put into test mode by opening switches to disconnect the top of the attenuators from the input pads. The test circuit can then be set to inject a current pulse into the attenuator by applying a positive 3v ECL signal. The amplitude of the current pulses range from 0-500mA in steps of 33mA which produce voltages at the 1kΩ attenuator input that range from 0-500mV in steps of 33mV.

4.2.3 Layout

The prototype 2 Magic layout is shown in Fig. 4.17. The VGA inputs are located along the left side of the die with the channels running horizontally across the chip. The tuning block is located on the right side of the die approximately half way down from the top.

The protection circuitry was modified to provide separate Vdd and Vgnd connections for the protection diodes at the inputs of each channel in an attempt to reduce the feed through and cross talk observed in the first prototype.

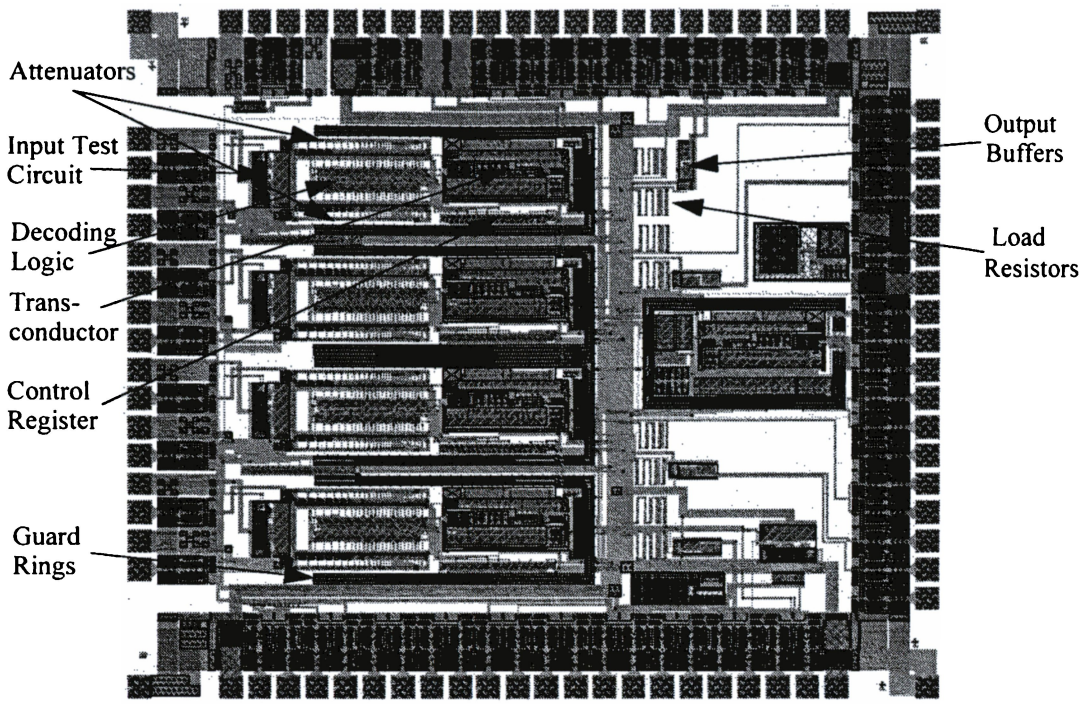


Fig.4.17 Prototype 2 Magic Layout.

Aggressive guard rings as shown in Fig. 4.18 were added to the channel to reduce any cross talk through the substrate and to isolate the channels from other on chip noise sources.

4.2.4 Prototype 2 Test Boards

Three test boards were constructed to evaluate the Prototype 2 chip. The DC board was used for the input and output resistance measurements, the test input amplitude measurements, and for the tuning current measurements. Testvga1_boardA was designed to allow testing of the unbuffered outputs and was used for the DC gain, offset, and linearity measurements. Testvga1_boardB was designed for testing the buffered outputs and was used for most of the AC testing. The construction technique developed for the Prototype 1 AC board using coaxial cables for the input and output signals was used for the Testvga1_BoardA and the Testvga1_BoardB boards. The DC board does not have input

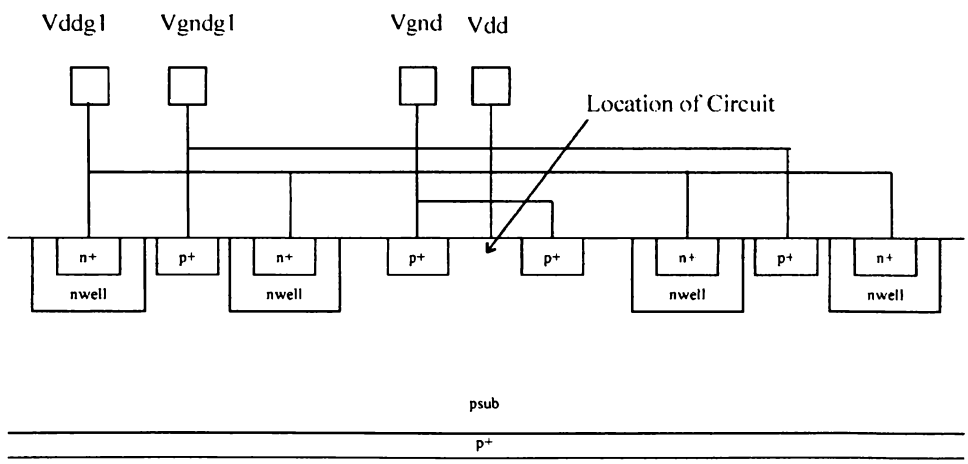


Fig.4.18 Guard Rings Used in Prototype 2.

and output connectors or termination. Because the socket for the prototype chip is a through-hole component, the boards are constructed with the socket on the bottom side of the board to allow short-lead-length connections to the supporting circuitry and the ground plane. Board A is shown in Fig. 4.19 and its schematic is shown in Fig. 4.20. Board A has eight input cables and eight output cables. The input cables are terminated with 50Ω resistors and the output cables are un-terminated. Board B is shown in Fig. 4.21 and its schematic is shown in Fig. 4.22. The buffered outputs drive off-chip 300Ω loads and a MAX 436 is used to perform a differential to single-ended conversion. The MAX 436 has a gain of 2 and a bandwidth of approximately 70MHz. An AD811 is used to provide an additional gain of 10. Back termination of the output cables results in a 0.5 gain loss due to voltage division. Thus the channel has an additional gain of 10 following the VGA.

4.2.5 DC Measurements

Offset

The transconductor offsets were measured by grounding both inputs of the transconductor by setting the gain code to zero and then measuring the differential output voltages (*Voutoff*) at the unbuffered output. A DC input signal was then applied and the output voltage (*Voutsig*) was measured with the channel set for zero attenuation. $Voutoff = AVos$ and $Voutsig = A(Vos + Vin)$, thus the channel gain can be eliminated by forming the ratio $K = (Voutsig)/(Voutoff) = \frac{Vos + Vin}{Vos}$. The input referred offset voltage is then calculated from the two measured output voltages using the equation $Vos = \frac{Vin}{K-1}$. The resulting input referred offset voltages are reported in Table 4.3.

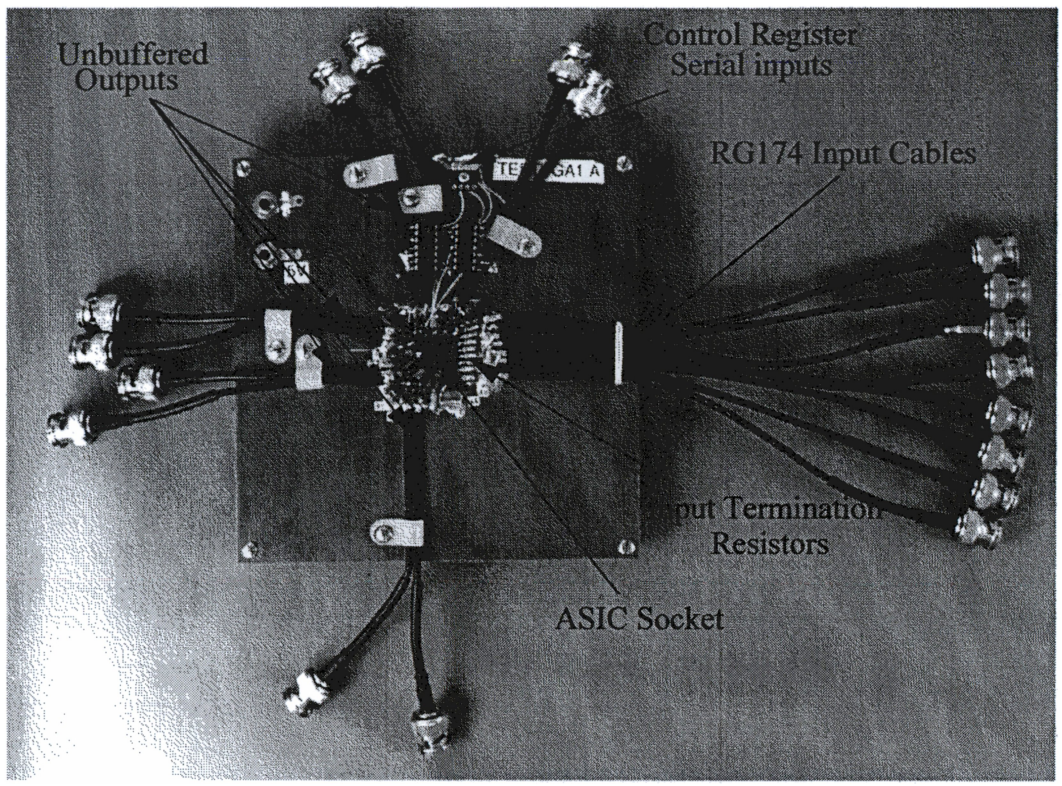


Fig.4.19 Testvga1_board A Test Board for Prototype 2.

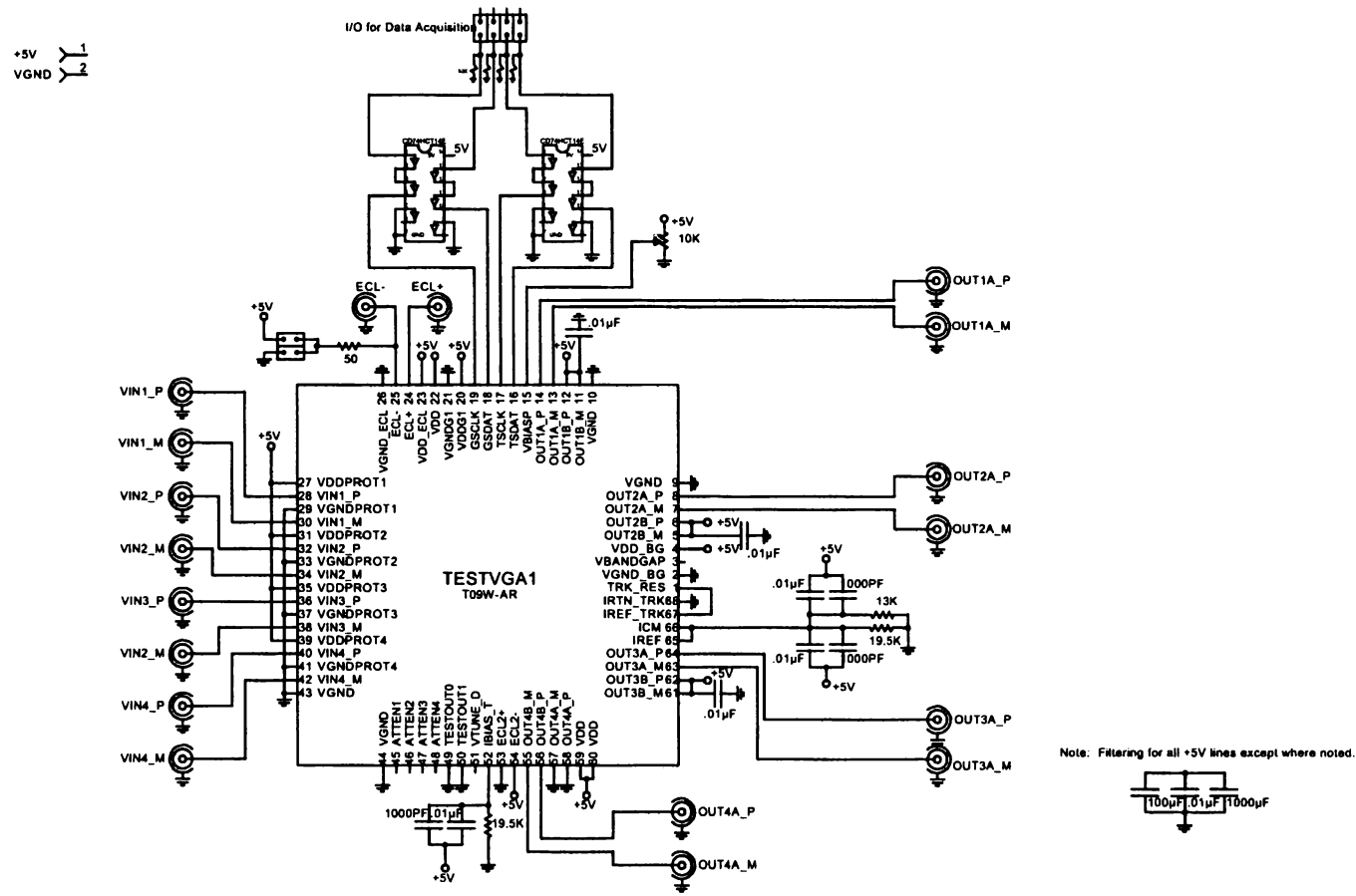


Fig.4.20 Testvga1_board A Schematic.

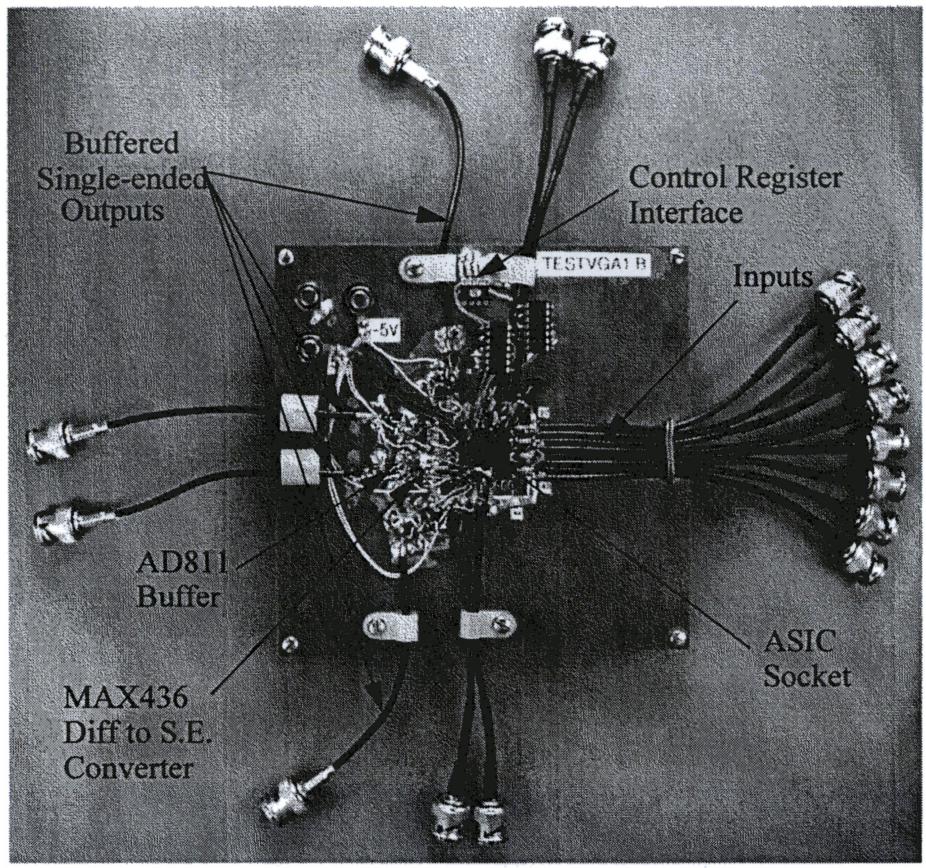


Fig.4.21 Testvga1_board B Test Board for Prototype 2.

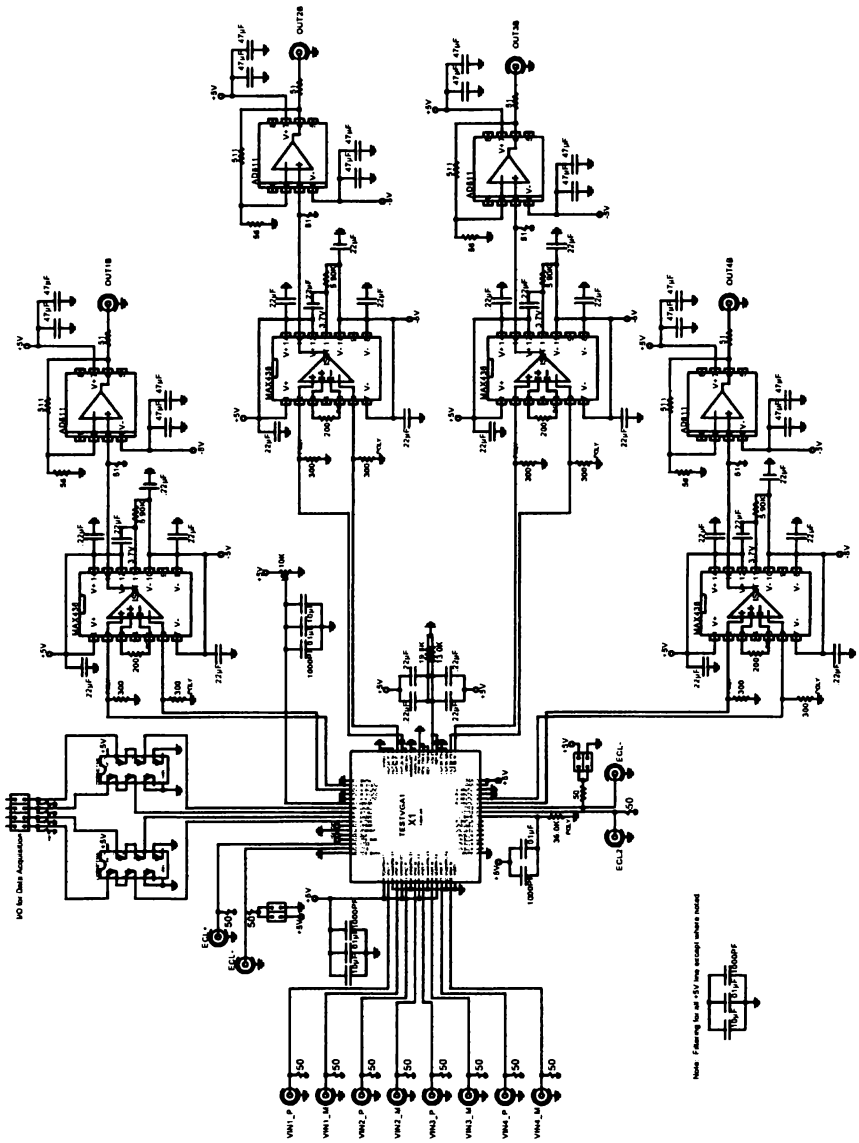


Fig.4.22 Testvga1_board B Schematic.

Table 4.3: Measured Input Offset Voltages for Prototype 2

Chip #	Chan. A (mV)	Chan. B (mV)	Chan. C (mV)	Chan. D (mV)
1	-2.92	0.44	-3.36	-2.00
2	-1.72	-0.34	-1.73	0.25
3	-1.30	-1.96	2.03	-3.02
4	-0.61	0.47	-4.06	-0.12
5	1.58	-0.09	-4.74	-3.89
6	-2.24	1.03	1.93	-0.10
7	4.32	-2.83	-1.21	4.25
8	0.65	-3.05	-1.46	-2.54
9	2.67	-1.31	-0.95	-1.96
10	1.76	-1.38	-0.07	-0.43
11	2.86	-0.84	0.12	0.64
12	0.37	-1.69	-3.92	0.05
13	-2.02	-1.78	-1.33	-1.52
14	1.76	-3.77	-0.53	-4.39
15	0.58	0.71	1.59	1.52

The measured input offset voltages were used to calculate the summary statistics and to plot the associated Gaussian distribution shown in Fig. 4.23. The mean of -0.693 mV is consistent with the expected zero mean. The Gaussian distribution is an estimate of the probability distribution function of the offset voltage and indicates a 3 sigma value of approximately 6mV which is comparable to the 5mV value measured for prototype 1. This 6mV 3 sigma value translates into a 3 sigma gain error of 12% in the slave transconductors, but affects all channels the same way on a given chip. Thus the gain error does not degrade the position information from the block detector attached to the chip, but merely results in a chip-to-chip gain variation.

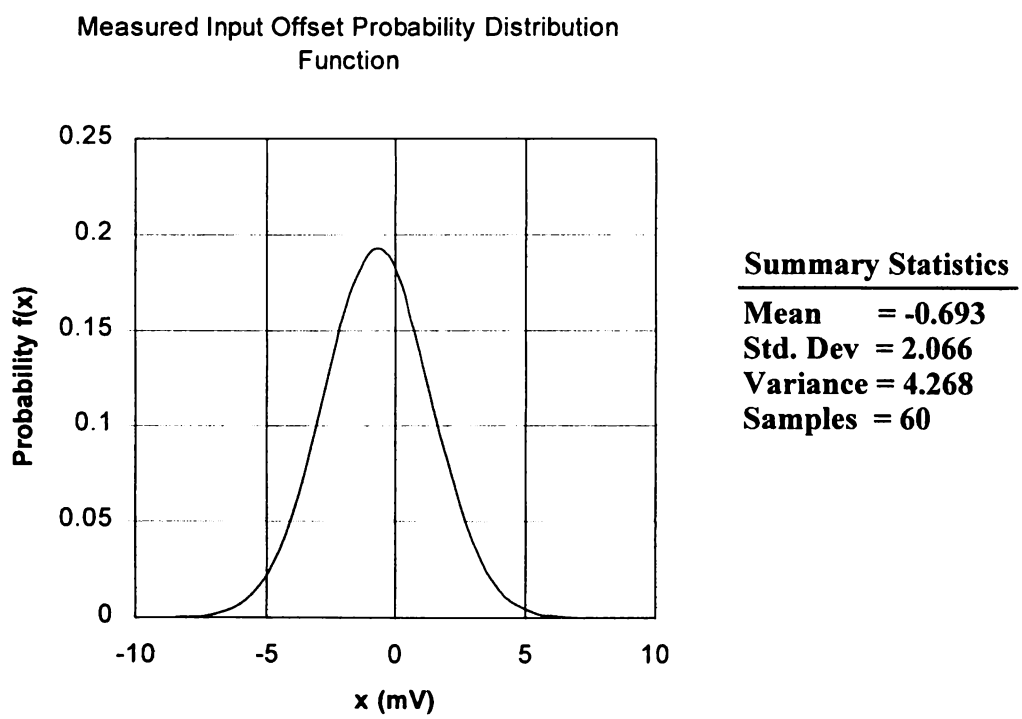


Fig.4.23 Gaussian Distribution of the Input Referred Offset Voltage for Prototype 2.

Gain Settings

The gain settings for the VGA were measured by applying a voltage at the input of the VGA and measuring the differential output voltage across the unbuffered outputs for each of the gain settings. Fig. 4.24 shows the raw gain data. The raw data was then offset corrected by subtracting the measured output offset voltage from the measured output voltage for each channel. The resulting gains are plotted in Fig. 4.25 on a linear scale and in Fig. 4.26 on a log scale to show the linear in dB nature of the gain steps. The average maximum gain is 9.66 v/v, which is reduced by 3.4% from the expected valued of 10 v/v. The gain reduction can have many contributing factors. Voltage division between the attenuator ladder and the ~10Ω input-enable switch accounts for approximately 1.5% of the gain reduction. Systematic mismatch between the on-chip tuning resistor and the on-chip load

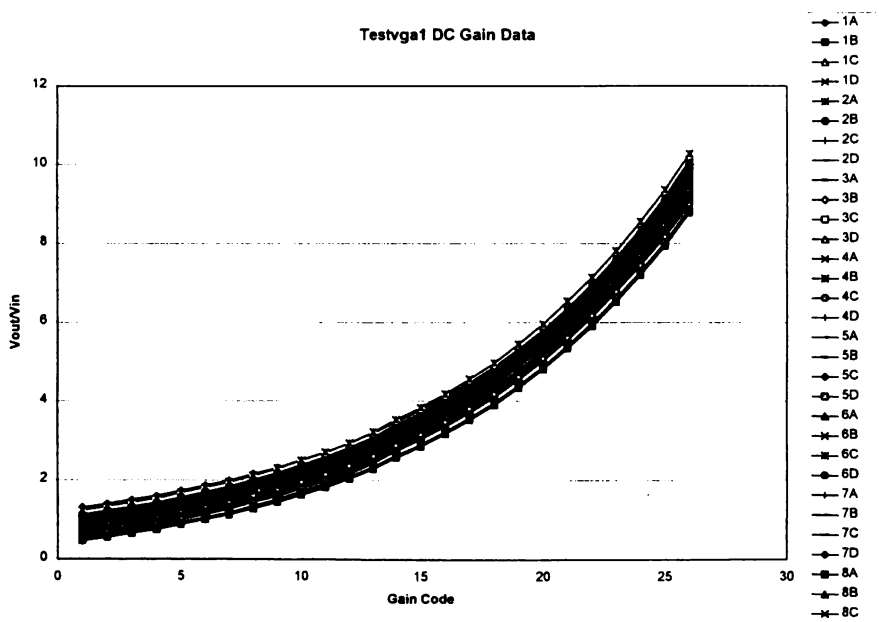


Fig.4.24 Gain vs. Gain Code - Raw Data.

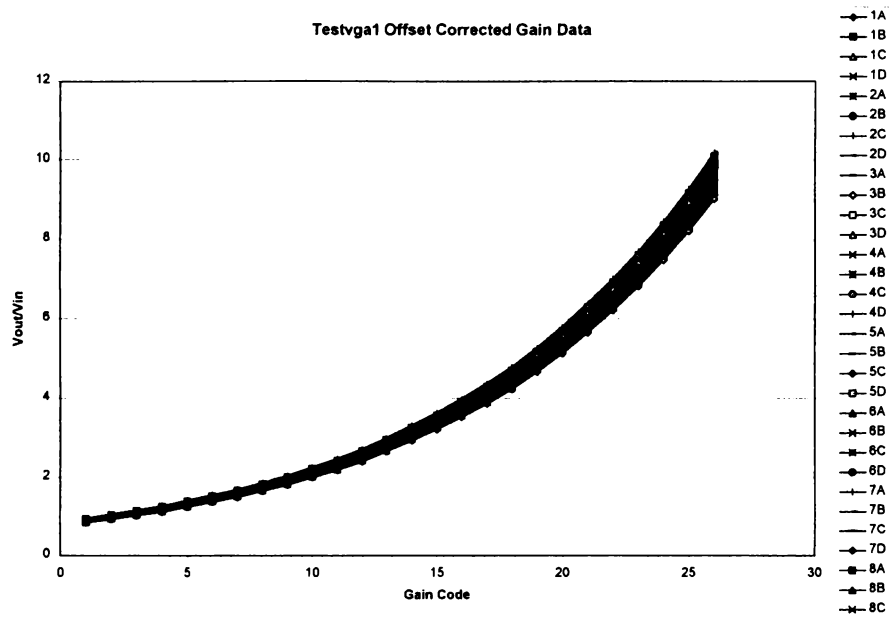


Fig.4.25 Gain vs. Gain Code - Offset Corrected.

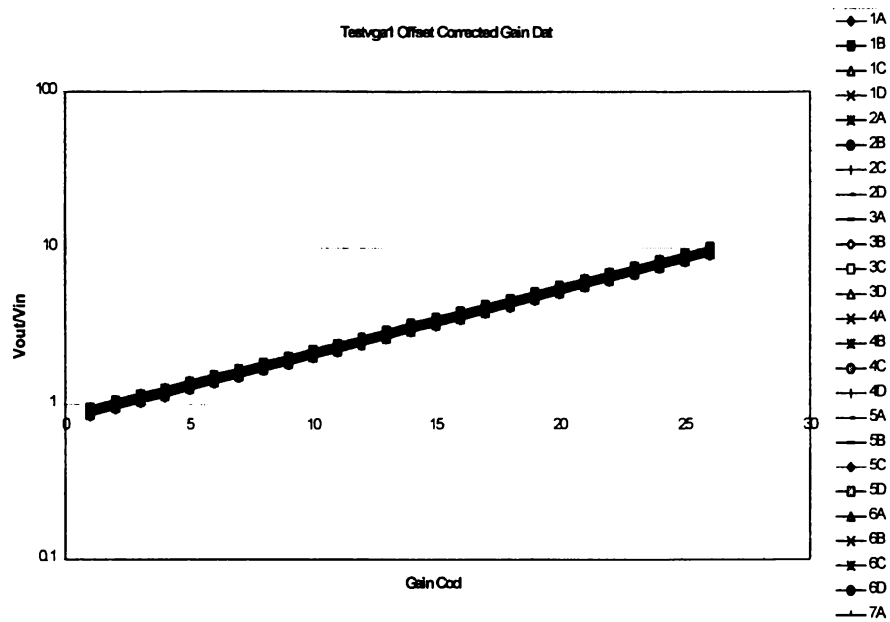


Fig.4.26 Gain vs. Gain Code - Offset Corrected, Log Scale.

resistors can account for the rest of the gain reduction. The maximum gain values were used to calculate the gain distribution for the transconductor. The summary statistics and corresponding gaussian distribution is shown in Fig. 4.27.

Linearity

The linear input range the transconductor was measured by setting the attenuator for maximum gain (no attenuation) and then sweeping the differential input voltage from -200mV to + 200mV and recording the differential output voltage as shown in Fig. 4.28. The response is very linear up to ± 150 mV, at this point the transconductor signal current is large enough to shut down one side of the output stage since it is as large as the common mode level but of opposite polarity.

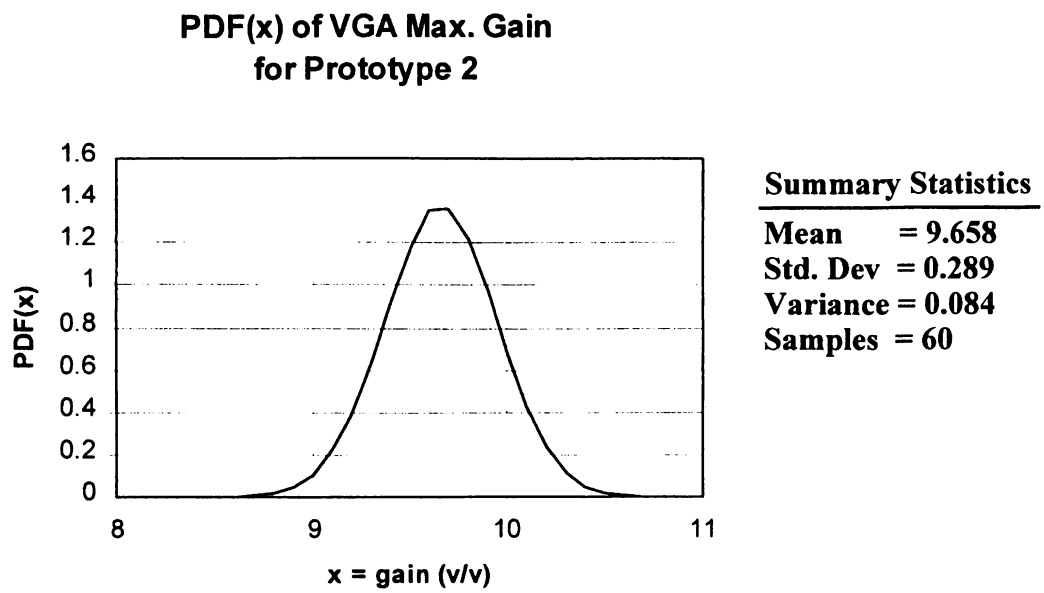


Fig.4.27 Gaussian Distribution of Maximum Gain for Prototype 2.

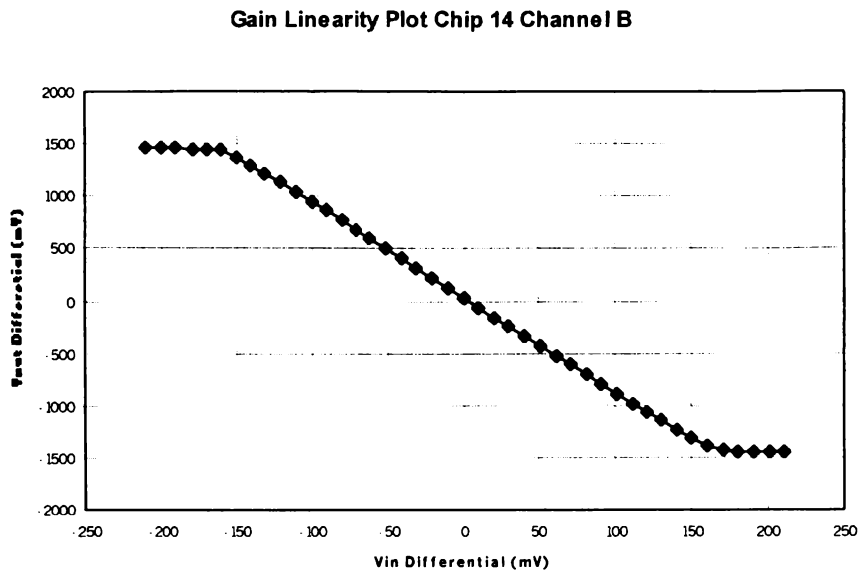


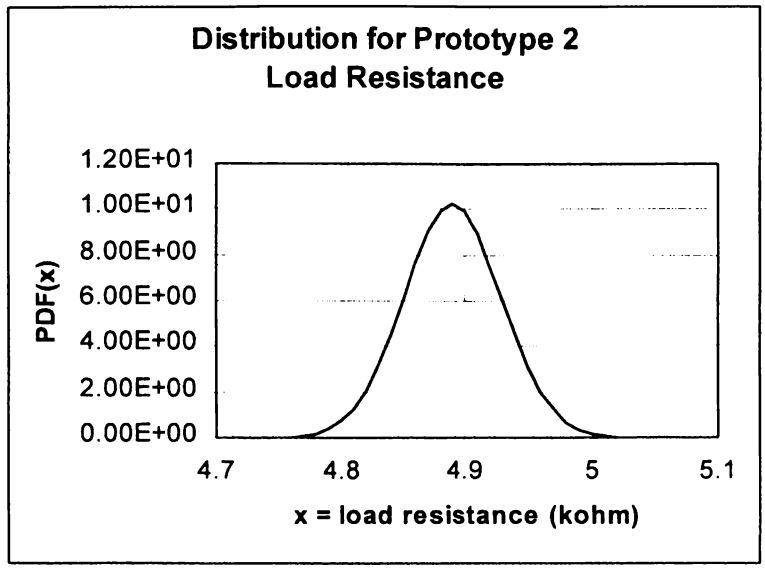
Fig.4.28 Linear Input Range Sweep.

Load Resistance

The load resistance was measured for each of the unbuffered outputs using a Keithly 2000 Multi meter as an ohm meter. The voltage produced in the measurement process was monitored for polarity and magnitude using a Fluke 79 III multi meter. The resulting resistance values are given in Table 4.4. The summary statistics and corresponding gaussian distribution for the load resistors is shown in Fig. 4.29. The distribution only represents the variation in load resistance for the prototype fabrication run and gives little insight into the true variation from run to run. A more useful measurement is the percent mismatch between the pairs of load resistors on each differential output. This distribution is shown in Fig. 4.30 along with the summary statistics and indicates a 3 sigma%-pair-mismatch of approximately 1.5 %.

Table 4.4: Measured Load Resistor Values

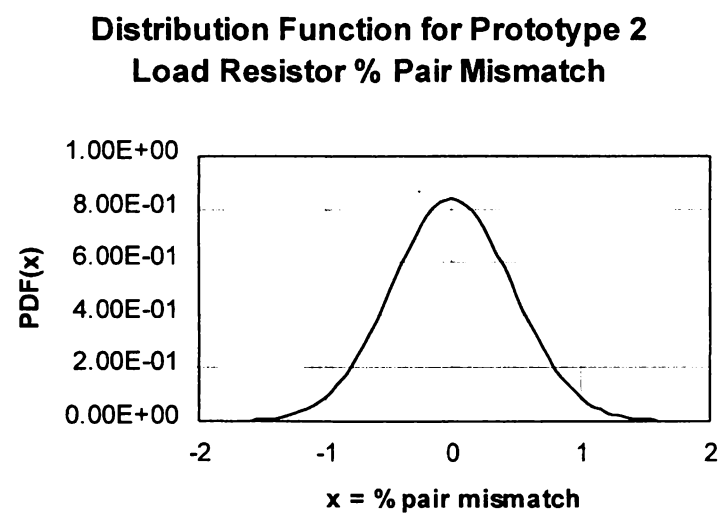
Chip #	$R_{load}A+$ (kΩ)	$R_{load}A-$ (kΩ)	$R_{load}B+$ (kΩ)	$R_{load}B-$ (kΩ)	$R_{load}C+$ (kΩ)	$R_{load}C-$ (kΩ)	$R_{load}D+$ (kΩ)	$R_{load}D-$ (kΩ)
1	4.903	4.863	4.908	4.913	4.924	4.912	4.903	4.913
2	4.902	4.873	4.919	4.942	4.903	4.899	4.915	4.885
3	4.911	4.934	4.985	4.977	4.963	4.98	4.96	4.952
4	4.862	4.859	4.898	4.905	4.908	4.885	4.891	4.902
5	4.821	4.846	4.867	4.857	4.888	4.857	4.863	4.848
6	4.785	4.784	4.817	4.854	4.831	4.832	4.839	4.829
7	4.879	4.804	4.976	4.937	4.906	4.916	4.907	4.929
8	4.852	4.871	4.894	4.906	4.914	4.885	4.911	4.888
9	4.863	4.857	4.904	4.943	4.925	4.915	4.89	4.929
10	4.836	4.859	4.905	4.878	4.884	4.899	4.888	4.87
11	4.838	4.842	4.881	4.894	4.872	4.876	4.887	4.883
12	4.886	4.862	4.915	4.917	4.937	4.908	4.909	4.891
13	4.852	4.837	4.871	4.872	4.836	4.878	4.86	4.848
14	4.895	4.932	4.881	4.876	4.89	4.924	4.849	4.862
15	4.878	4.888	4.938	4.94	4.93	4.945	4.887	4.915



Summary Statistics

Mean = 4.890
Std. Dev = 0.039
Variance = 0.0015
Samples = 120

Fig.4.29 Gaussian Distribution of Prototype 2 Load Resistance.



Summary Statistics

Mean = -0.005
Std. Dev = 0.475
Variance = 0.225
Samples = 60

Fig.4.30 Gaussian Distribution for Prototype 2 Load Resistor% Pair Mismatch.

Input Resistance

The input resistance was measured for each input of the VGA channels using a Keithly 2000 Multi meter as an ohm meter. The voltage produced in the measurement process was monitored for polarity and magnitude using a Fluke 79 III multi meter. The measurements could only be performed with the input switches enabled and thus the measured resistances include the on-resistance of the switches which is approximately 10Ω. The resulting resistance values are given in Table 4.5, and the associated statistics are shown in Fig. 4.31.

Input Test Amplitudes

A block diagram of the VGA including the input test circuit is shown in Fig. 4.32. The input test amplitudes were measured by enabling the input switches and applying an ECL logic signal to activate the pulse generator. The resulting voltages produced at the VGA inputs are shown in Fig. 4.33. The curves are very linear and the maximum value of 450 mV is consistent with the measured reference current of 98 uA and the attenuator resistance of 920 Ω. In the production chip the reference current will be tuned to polysilicon so that the current will be higher than the nominal value for low polysilicon resistance values resulting in better regulation of the input test amplitudes. Fig. 4.34 a.) shows the resulting VGA output for a sweep of the test amplitude codes and b.) shows the output perturbation of the VGA due to charge injection associated with the switches M1-M2 in the test circuit shown in Fig. 4.35. The production version of the test input should use a capacitor C1 connected to the opposite phase of the test pulse signal to compensate for the charge injection of M2.

Table 4.5: Measured Input Resistances for Prototype 2

Chip #	RinA+ (Ω)	RinA- (Ω)	RinB+ (Ω)	RinB- (Ω)	RinC+ (Ω)	RinC- (Ω)	RinD+ (Ω)	RinD- (Ω)
1	937	933	935	936	935	935	937	935
2	934	933	935	934	934	931	934	933
3	938	934	940	938	936	937	938	934
4	934	932	932	934	935	933	934	932
5	931	930	931	932	929	927	929	928
6	915	915	917	915	915	912	916	916
7	935	933	936	935	935	932	937	934
8	932	929	929	932	934	930	934	934
9	936	933	934	936	934	935	932	934
10	931	928	934	932	930	930	936	933
11	929	930	933	933	932	930	933	929
12	935	931	935	934	936	933	931	933
13	928	926	929	928	926	924	927	924
14	936	934	935	932	933	935	933	932
15	935	930	937	934	935	934	937	935

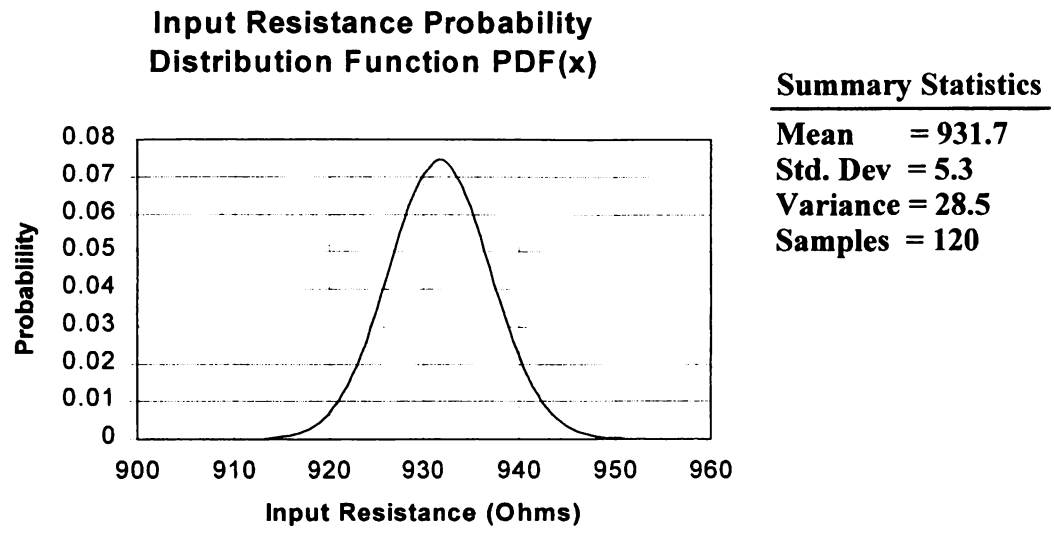


Fig.4.31 Gaussian Distribution for Prototype 2 Input Resistors.

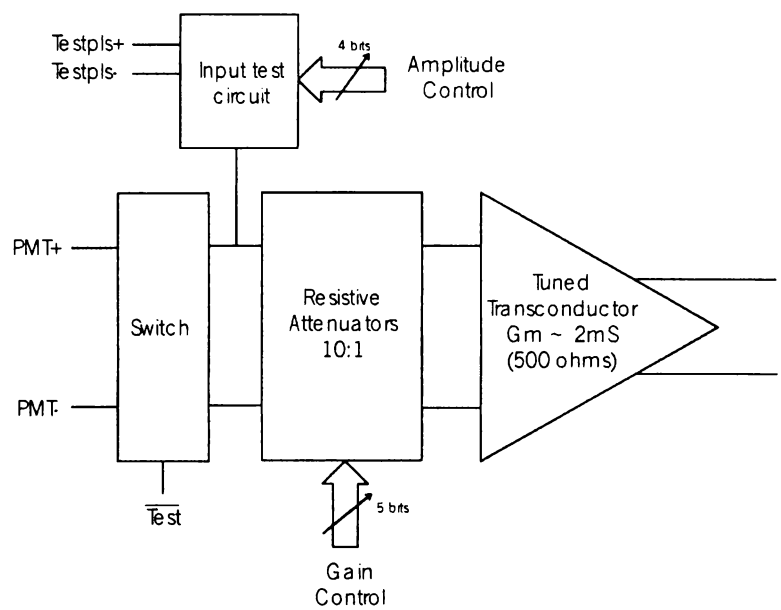


Fig.4.32 VGA Block Diagram Showing Input Switches and Input Test Circuit.

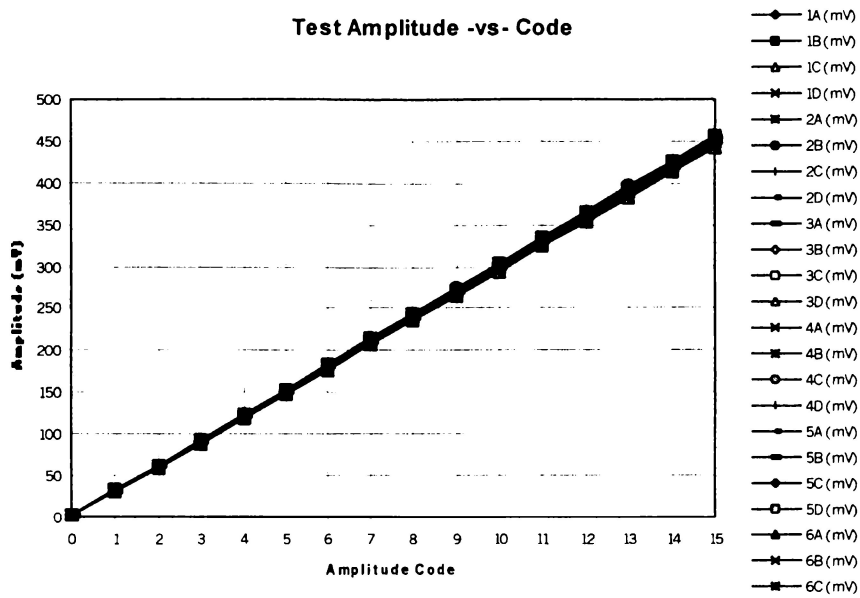


Fig.4.33 Input Test Voltages -vs.- Amplitude Code.

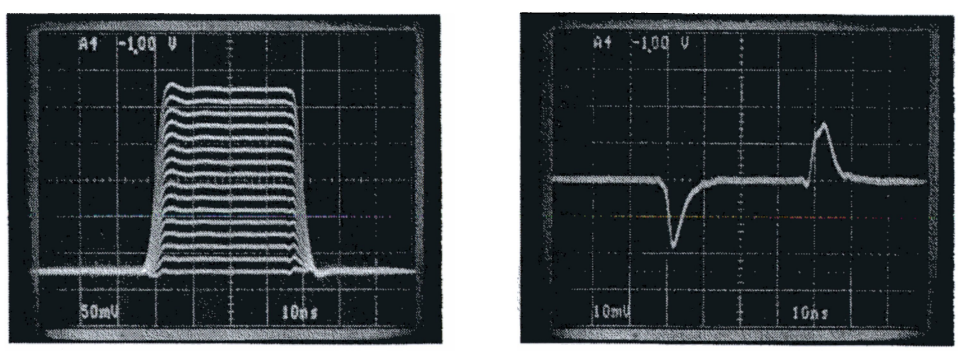


Fig.4.34 Input Test Voltage a.) Amplitude Code Sweep and b.) Charge Injection.

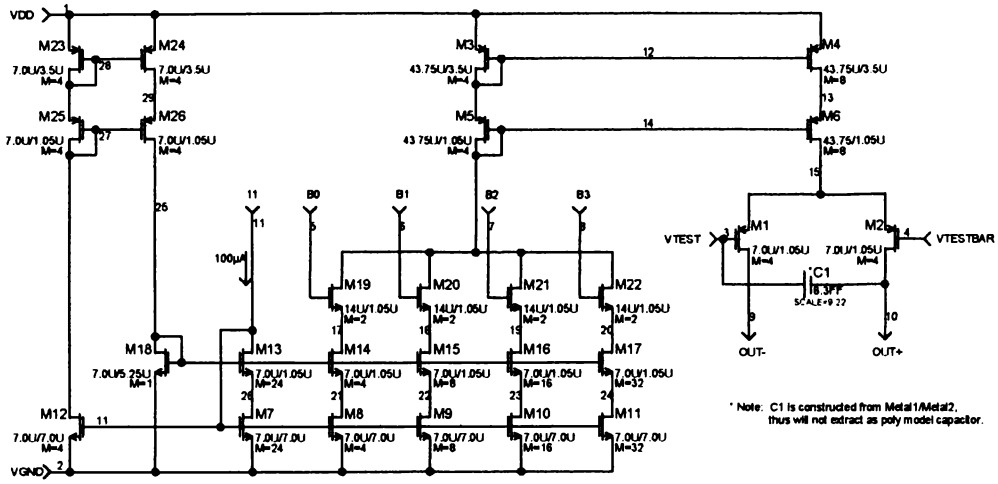


Fig.4.35 Input Test Circuit Schematic with Added Charge Injection Cancellation Capacitor C1.

Tuning Range and Startup

Five of the fifteen chips tested started up with the tuning loop in a latched-up state. By adding a capacitor from the positive input of the tuning transconductor (pin 67, Fig. 4.20) to Vdd, the voltage across the tuning resistor is forced to a large value that decays with a long time constant. Thus the tuning loop is forced to start with a small tuning current and to gradually increase the current to the desired value. This forces the tuning loop into the correct operating condition for all 15 of the chips. The chips that had difficulty starting up also had slightly larger gains, which is consistent with a negative offset voltage in the master transconductor resulting in a lower effective tuning voltage and thus a larger tuned transconductance. This problem and a possible solution are discussed in chapter 3.

4.2.6 AC Measurements

Gain Steps

The gain steps for the buffered output are shown in Fig. 4.36. The gain of the buffers is approximately 1/2 resulting in a max gain of approximately 5 V/V. The photograph is a multiple exposure with the buffered output shown for a 50 mV input signal and a sweep over the gain settings.

Risetime/Bandwidth

A 1ns rise-time HP 8082A pulse generator and a 350MHz Tektronix 2465A oscilloscope were used to observe the risetime and overshoot of the buffered output in response to a 1ns risetime input pulse. The risetime at the output of the on-chip buffer was 3.4 ns indicating a bandwidth of approximately 103 MHz. The risetime at the output of the MAX436 was degraded to 5.8 ns indicating the bandwidth for the converter of 75 MHz and a composite bandwidth of 60 MHz. The output of the AD811 was even further degraded to 8.4 ns which indicates the amplifier has a bandwidth of 60 MHz resulting in a

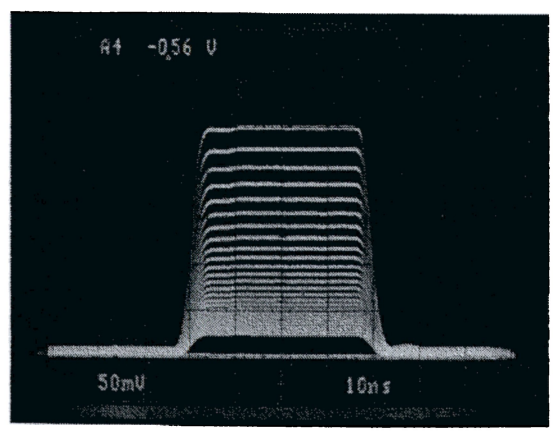


Fig.4.36 Gain Code Sweep for a 50mV input signal using the buffered outputs with a max gain of ~ 5 v/v.

composite bandwidth for the complete test channel of approximately 40MHz. The simulated bandwidth of the buffered outputs was approximately 150MHz and thus the 100MHz experimental value was unexpected. Further investigation suggests that the parasitic capacitances associated with the on-chip 5k load resistors are not properly modeled and that the extra capacitance is degrading the bandwidth performance of the circuit. This implies that the production version of the loads should be constructed using the high resistance polysilicon layer to maintain the proper bandwidth.

The magnitude of the test channel transfer function was measured using the HP3589A Network Analyzer. The results shown in Fig. 4.37 are consistent with the risetime measurements and indicate a bandwidth of approximately 40MHz.

The bandwidth of the unbuffered outputs was measured by observing the ristime for the output signals when the outputs are AC coupled to the 50Ω inputs of the oscilloscope and a 1 ns ristime pulse is applied to the input. Fig. 4.38 shows the measured risetimes vs. gain setting for all four channels of chip 1. The maximum of 2.85 ns can be corrected to account for the ristime of the scope and pulser to give 2.47 ns or a bandwidth of 140 MHz. This result is consistent with the theory that the parasitic capacitances of the polysilicon resistors are not modeled correctly and the bandwidth of the buffered outputs is being degraded by the bandwidth of the load resistors.

Delay Dispersion

The delay dispersion over the gain range was measured by choosing the maximum gain setting as the reference delay and observing the time shift of the signal mid-point as the gain was adjusted over the full scale. The test was performed using Testvga1_Board A

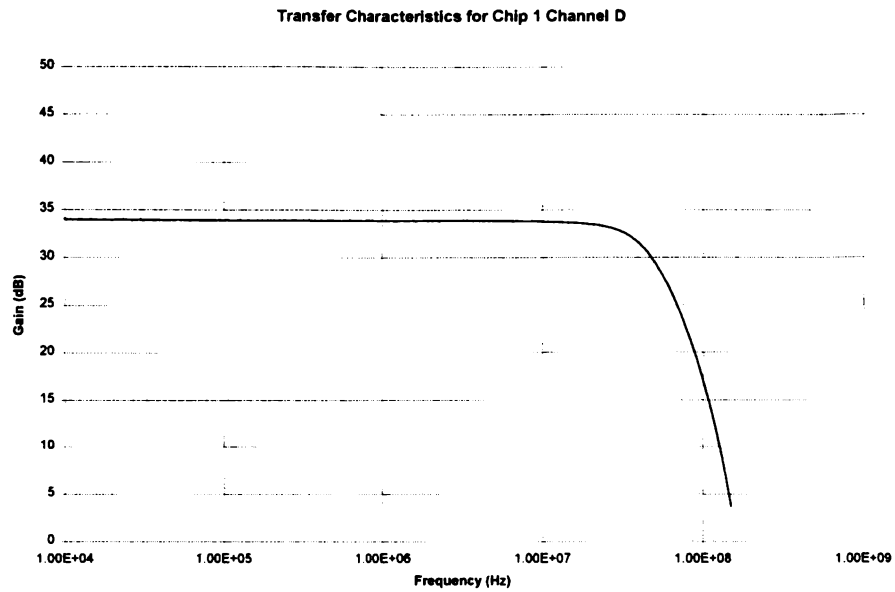


Fig.4.37 Testvga1_BoardB Transfer Function Magnitude.

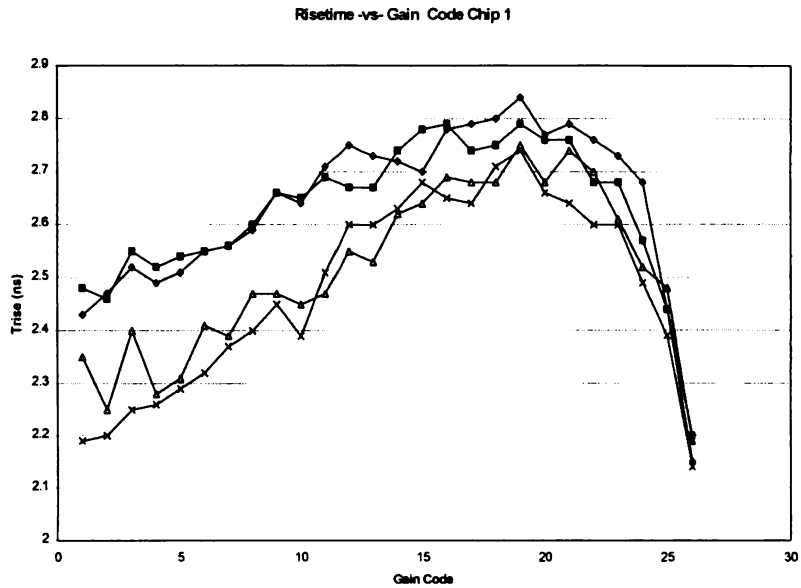


Fig.4.38 Testvga1_BoardA Unbuffered Output Risetime Measurements.

with a Techtronix 2465A oscilloscope used to perform the differential to single-ended conversion. The amplitude of the input signal supplied by the HP 8082A pulse generator was adjusted using high frequency attenuators to maintain an output signal level that could be observed without adjustment of the oscilloscope or the pulse generator. The delay of the attenuators used to perform the test was measured to be less than 50ps. The equipment for the dispersion testing allowed a measurement accuracy of approximately +/- 100ps for the delay data. As shown in Fig. 4.39, the measured delay shift increased to a maximum value of ~500 ps at the gain code of 15 and then decreased to 200 ps as the gain was reduced further resulting in a maximum delay dispersion of slightly less than 500 ± 100 ps which is will within the specified 1 ns maximum.

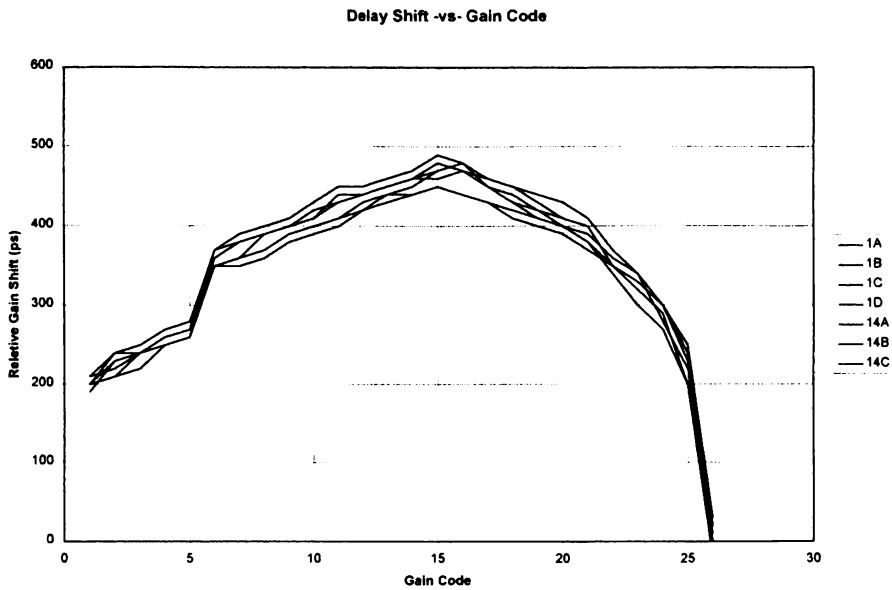
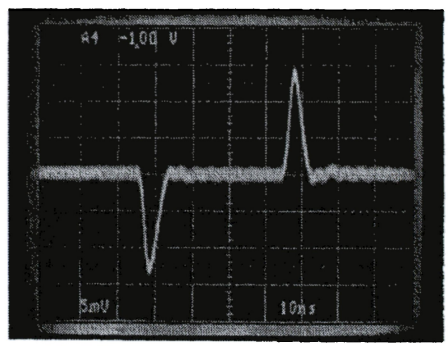


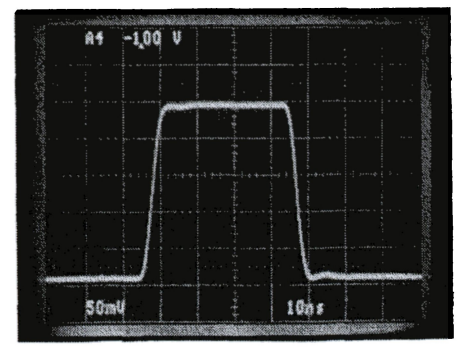
Fig.4.39 Delay Dispersion -vs.- Gain Code.

Crosstalk

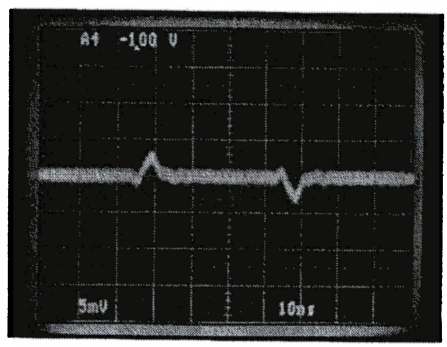
Channel to channel crosstalk was evaluated by applying a 500mV input signal to the input of one channel set for minimum gain and observing the output of the adjacent channels set for maximum gain. A typical set of images is shown in Fig. 4.40 in which a 500mV signal is applied to channel B and the outputs for all four channels are recorded. The largest crosstalk occurs between channels with adjacent inputs, in this case between channel A and channel B. The 15mV peak output signal produced by the crosstalk is approximately 6% of the typical peak output signal level and thus is acceptable for the intended application, however, a reduction in the crosstalk level is desirable. The source of the majority of the channel to channel coupling is most likely in the packaging and test



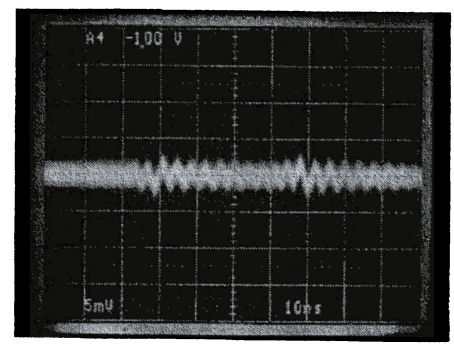
Channel A Max. Gain



Channel B Min. Gain



Channel C Max. Gain



Channel D Max. Gain

Fig.4.40 Crosstalk Photographs for Prototype 2.

socket, both of which will be different in the production version. Thus the crosstalk characteristics of the production version are difficult to predict. The crosstalk between a logic pulse and the VGA, which was a concern in the first prototype, has been greatly improved in the second protoype as can be seen in Fig. 4.41. In this figure, a 4 volt "logic" signal is applied to an on-chip test resistor with a distance from the VGA input and resistance value similar to the resistor used in the prototype 1 test. Prototype 2 shows significant improvement in this test.

CMRR

The common mode rejection ratio for prototype 2 was measured for a buffered channel by first using the configuration shown in test 1 of Fig. 4.42 a.) to determine the gain from Vin differential to Vo2. The output voltage is given by

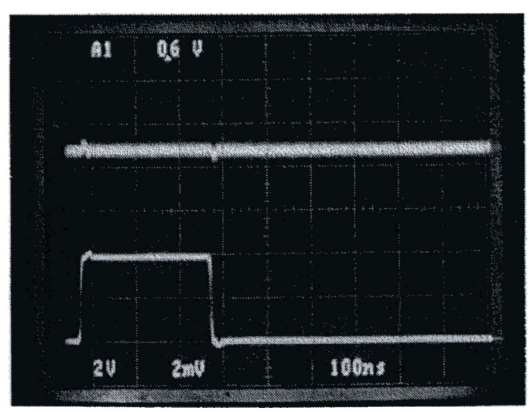
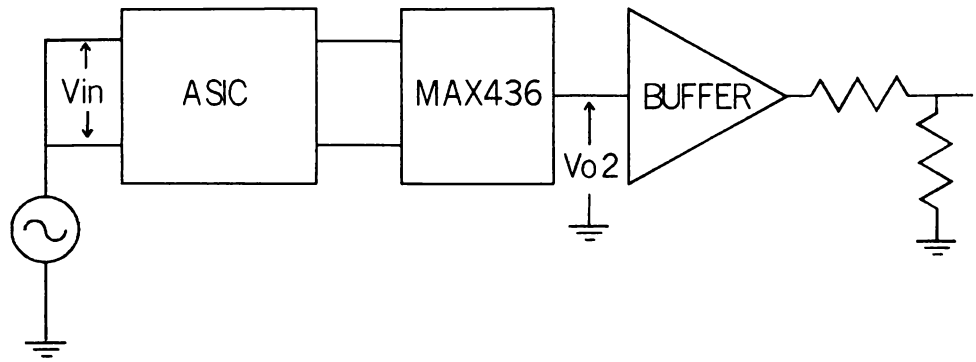
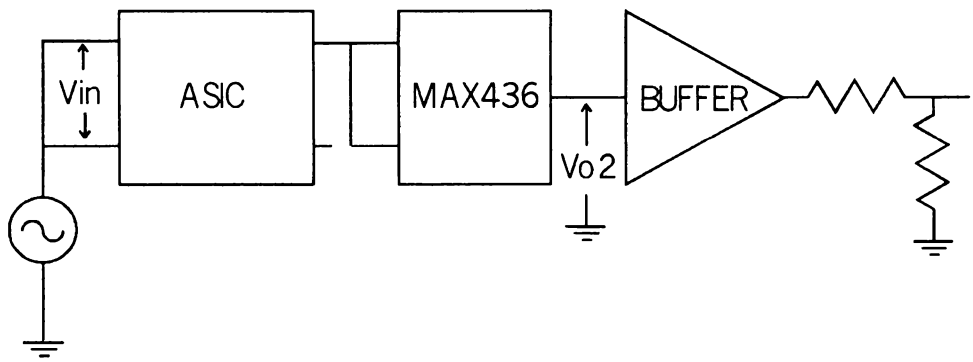


Fig.4.41 Crosstalk Photographs for Prototype 2.



a.) Test #1



b.) Test #2

Fig.4.42 CMRR Measurement for Prototype 2.

$$Vo2 = V_{incm}((A_{cm}|_{conv})(V_{ocm}|_{chip}) + (A_{dm}|_{conv})(V_{od}|_{chip}))$$

where the first term is due to the CM output of the chip and the CM gain of the MAX436 differential to single-ended converter and the second term is due to the differential output of the chip and the differential gain of the MAX436. V_{incm} is the common-mode input voltage applied to the chip, A_{cm} is the common mode gain of the differential-to-single ended converter, A_{dm} is the differential mode gain of the differential-to-single ended con-

verter, and V_{ocm} and V_{od} are the CM and differential mode output voltages of the chip respectively. Test 2 shown in Fig. 4.42 b.) was then performed to determine the value of the first term of the above expression. For this second configuration the output voltage is given by

$$Vo2 = V_{incm}(A_{cm}|_{conv})(V_{ocm}|_{chip})$$

where the output is due to the CM output of the chip and the CM gain of the MAX436. The resulting data is shown in Fig. 4.43. The data at lower frequencies for test #2 was very noisy and was thus approximated by the its average value of -75 dB. The differential gain of the MAX436 is given as a function of frequency in the data sheet [55], thus with

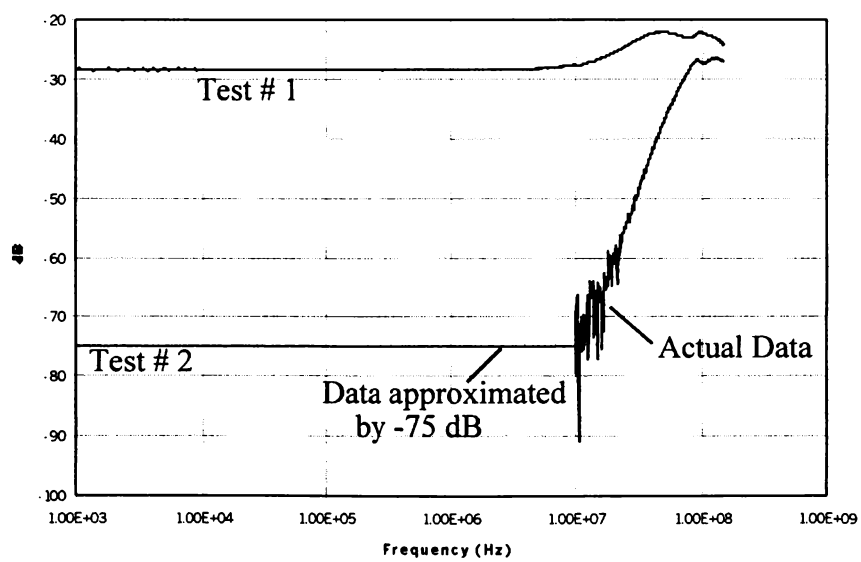


Fig.4.43 CMRR Data for Prototype 2.

the above tests, $V_{od}|_{chip}$ can be determined. The common mode gain of the chip defined as differential output voltage due to a CM input voltage is given by

$$A_{cm}|_{chip} = \frac{V_{od}}{V_{incm}}\bigg|_{chip} = \frac{|V_{o2(test1)}| \pm |V_{o2(test2)}|}{(A_{dm}|_{conv})V_{incm}}$$

since the relative phases of the terms are not known, the result is best stated in terms of worst and best case. The best case corresponds to the difference of the two magnitudes and the worst case corresponds to the sum of the two magnitudes. Both cases are shown in Fig. 4.44. In either case the CMRR is better than -45 dB which is approximately 35 dB better than is required by the specifications. Thus the CM noise rejection of the VGA at 100 MHz should be more than adequate for the application.

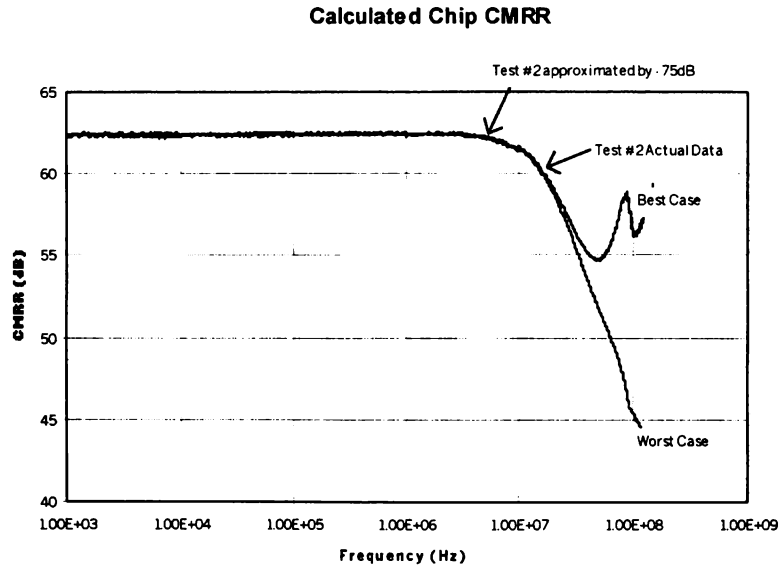


Fig.4.44 CMRR for Prototype 2.

Noise

The VGA channel noise spectrum was measured using an HP3589A spectrum analyzer and Testvga1_boardB. The noise floor of the analyzer is approximately 32 nV/rt-Hz thus the test board has an additional gain of 10 following the chip to raise the output noise up to a level that can be measured by the spectrum analyzer. Based on simulation results, the expected output noise of the VGA is approximately 35 nV/rt-Hz. The MAX436 acting as the differential to single-ended converter has an equivalent input noise of 7 nV/rt-Hz. which is not correlated to the output noise of the chip and thus combines in quadrature with the chip output noise to yield 35.7 nV/rt-Hz at the input of the MAX436. Thus the output noise of the MAX436 is 71.4 nV/rt-Hz. The MAX436 is followed by an AD811 that is configured for a gain of 10 and has a 1.9 nV/rt-Hz equivalent input noise which combines with the noise on the signal to produce a noise level of 714 nV/rt-Hz at the output of the gain stage. The output of the AD811 is 50Ω back terminated resulting in a 50% loss in gain with the cable connected to the 50Ω input of the spectrum analyzer. Thus, the expected noise at the input of the analyzer is approximately 357 nV/rt-Hz which is approximately 10 times as large as the noise floor of the analyzer. Using this test configuration, the output noise spectrum was measured and then was referred to the input of the transconductor using the measured channel gain. A typical measured input referred noise spectrum for the maximum gain setting is shown in Fig. 4.45 and corresponds well with the simulated input referred noise spectrum shown in Fig. 4.46. The flicker noise corner is at approximately 100 kHz and the white noise level is approximately 6.8 nV/rt-Hz. The white noise increases slightly for other gain settings with the maximum of 7.8 nV/rt-Hz at a gain setting of 17 as shown in Fig. 4.47. The increase in white noise can be explained by

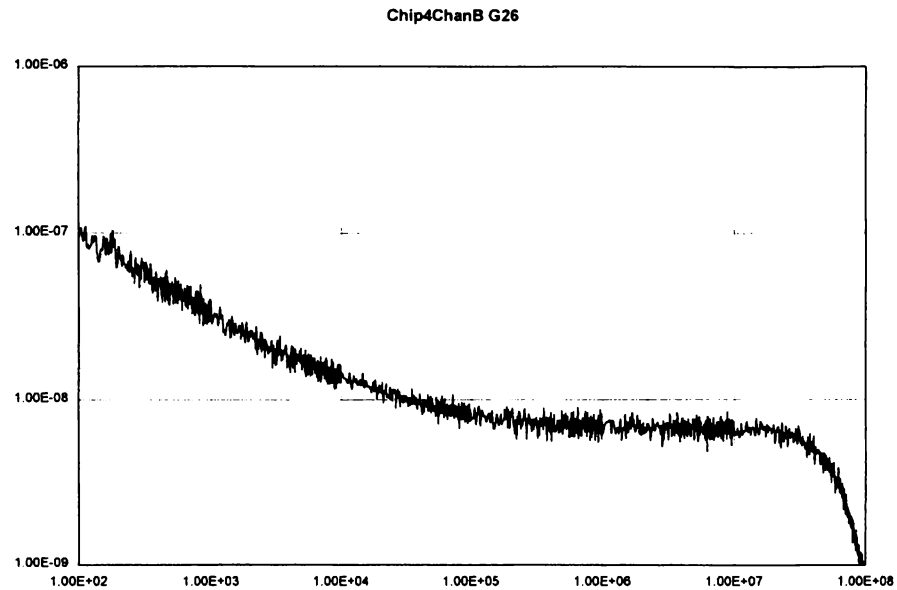


Fig.4.45 Measured Input Referred Noise Spectrum for Maximum Gain Setting.

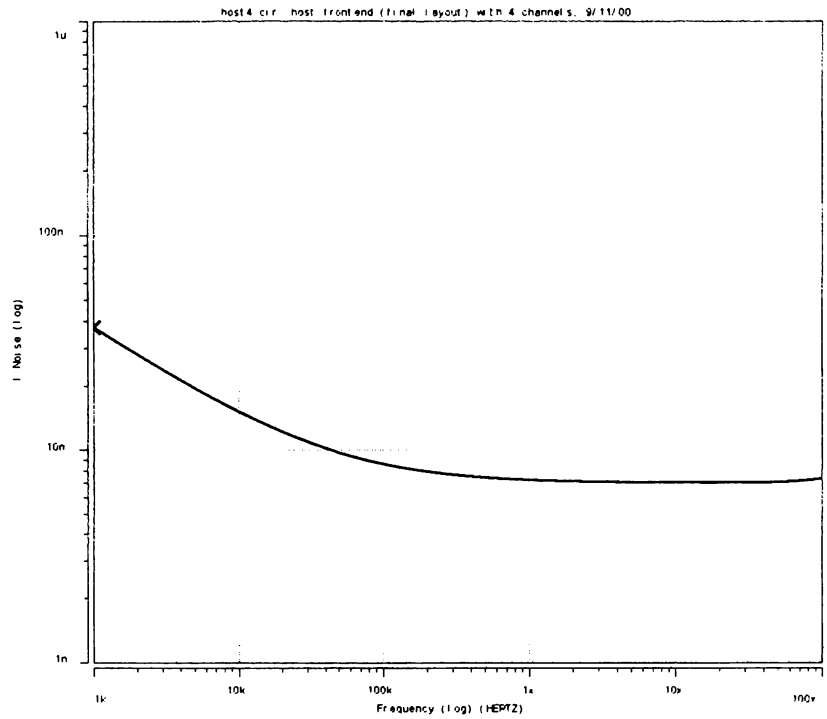


Fig.4.46 Simulated Input Referred Noise Spectrum for Maximum Gain Setting.

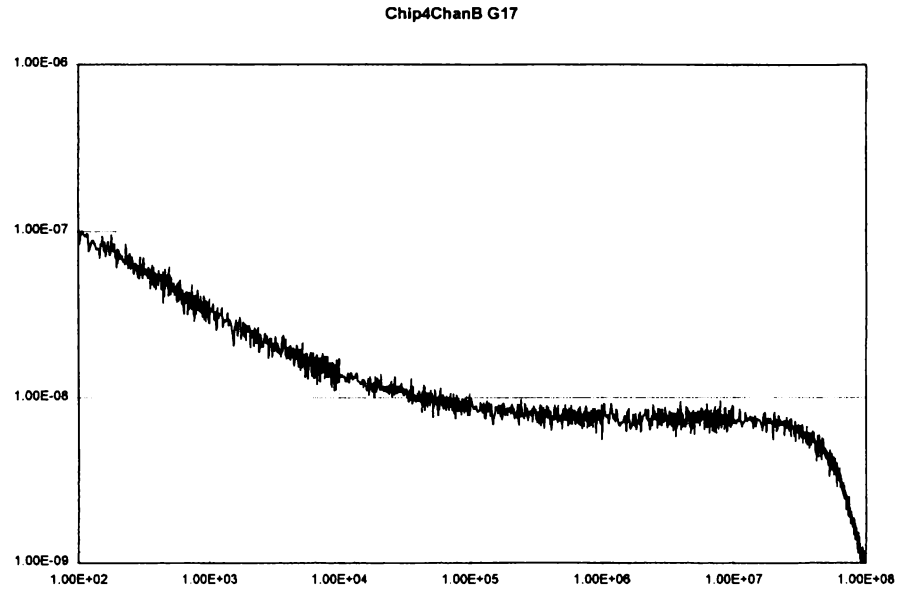


Fig.4.47 Measured Input Referred Noise Spectrum for Mid-Gain.

the higher thevenin resistance of the attenuator for the mid-gain settings and matches well with the theoretical noise increase discussed in Chapter 3. The measured noise corresponds very well with the simulated values and the white noise level is well below the specified 10 nV/rt-Hz, allowing for additional noise due to the summing and CFD stages.

4.2.7 Prototype 2 Conclusions

The data from prototype 2 shows that the modified continuous polysilicon attenuator based VGA has sufficient bandwidth and gain accuracy to meet the requirements of the Phase II ASIC. The bandwidth of the attenuator and transconductor combined is in excess of 140 MHz which is well above the required 100 MHz required for the system. The gain settings are monotonic and predictable, and the tuning scheme appears to be effective and

stable once the correct operation condition is established. The feed through and logic crosstalk observed in prototype 1 were reduced significantly, and the four channels allowed evaluation of channel to channel crosstalk. The magnitude of the channel to channel crosstalk is acceptable, but larger than desired. However, due to the change in packaging for the production version of the ASIC, the crosstalk characteristics of the production version are difficult to predict, and the layout and bonding of the production version should be carefully considered. Start-up of the tuning loop is another issue that must be resolved for the production version. The tuning loop in several of the prototype chips exhibited bi-stable operation resulting in the need for an external startup circuit. The production version should be modified so that the external startup circuit is not necessary. Except for these issues the prototype appears ready for production.

Chapter 5 Conclusions

5.1 Summary

This paper presented the design and analysis of an attenuator-based, integrated, four-channel, differential, 150 MHz, linear-in-dB VGA with sub-nanosecond delay dispersion. The design was developed as a component for the proposed Phase II ASIC for use in PET medical imaging systems. The basics of PET, a description of the Phase I ASIC, and the need for the Phase II ASIC are described in chapter 1. The specifications for the VGA are also given at the end of chapter 1. Next, a brief literature review of relevant VGA architectures is presented in chapter 2. The selected architecture for the Phase II VGA is then presented in chapter 3, and the design and analysis of each of the VGA compounds is discussed. Chapter 4 presents experimental results for two prototypes. Prototype 1 investigated the general suitability of the selected architecture. The design functioned well, but had some problems with feed through and crosstalk. Prototype 2 improved some of the high frequency crosstalk and feed through problems observed in the first prototype through the use of improved layout techniques. The design was found to have a start-up problem in the tuning loop which must be corrected before production, otherwise the circuit meets the required specifications and is ready for production.

5.2 Future Work

The primary area requiring future work before the design is ready for production is the start-up issue in the tuning loop discussed in chapter 3.

Future work of academic interest could include a numerical solution of the three dimensional, partial differential equations describing the voltage potential in the polysilicon attenuator structure. This analytical solution could be compared to the results of the one dimensional, distributed model used in this work and the validity of the model could determined. If the one dimensional model is insufficient, a more suitable model might be developed for use in SPICE simulation. One possible approach could be the development of a two dimensional resistor-capacitor network which should allow the asymmetry of the structure due to the taps to be modeled.

Bibliography

Bibliography

[1] J. M. Ollinger, and J. A. Fessler "Positron-Emission Tomography," IEEE Signal Processing Magazine, pp.43-55, Jan. 1997.

[2] M. E. Phelps, J. C. Mazziotta, and H. R. Schelbert, Positron Emission Tomography and Autoradiography, New York: Raven Press, 1986.

[3] Hamamatsu Photonics Editorial Committee, Photomultiplier Tube, Principle to Application,USA, Hamamatsu Photonics K.K., 1994.

[4] W.R. Leo, Techniques for Nuclear and Particle Physics Experiments, New York: Springer-Verlag, 1994.

[5] Sears, Zemansky, and Young, University Physics, 7th Ed., Reading, MA: Addison-Wesley, 1987.

[6] www.bicron.com/BGO.htm, Bicron Incorporated, April 2001.

[7] D.M. Binkley, J.M. Rochelle, M.J. Pualus, M.E.Casey, R. Nutt, W. Loeffler, and J.C. Moyers, "A Custom CMOS Integrated Circuit for PET Tomograph Front-End Applications," Conference Record of the IEEE 1993 Nuclear Science Symposium and Medical Imaging Conference, pp. 867-871, 1993.

[8] E. Tapscott, "Nuclear medicine pioneer: Hal O. Anger. First scintillation camera is foundation for modern imaging systems." Journal of Nuclear Medicine. 39:15n 1998.

[9] D.M. Binkley, Analysis and Development of Non-Delay-Line Constant-Fraction Discriminator Circuits, Including a Fully-Monolithic CMOS Implementation, Ph.D. Dissertation, University of Tennessee, Knoxville, 1992.

[10] J.C. Moyers, A High Performance Detector Electronics System for Positron Emission Tomography," Masters Thesis, University of Tennessee, Knoxville, May 1990.

[11] CTI Small Business Innovative Research PhaseII Grant Application, CTI inc., 1990.

[12] P. R. Gray, and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, New York: Wiley, 1993.

[13] T. Pan, and A. A. Abidi "A 50-dB Variable Gain Amplifier Using Parasitic Bipolar Transistors in CMOS," IEEE Journal of Solid-State Circuits, vol. 24, no.4, pp.951-961, August 1989.

[14] D. M. Pietruszynski, J. M. Steininger, and E. J. Swanson, "A 50-Mbit/s CMOS Monolithic Optical Receiver," IEEE Journal of Solid-State Circuits, vol. 23, no.6, pp.1426-1433, Dec. 1988.

[15] W. M. C. Sansen, and R. G. Meyer, "An Integrated Wide-Band Variable-Gain Amplifier with Maximum Dynamic Range," IEEE Journal of Solid-State Circuits, vol. SC-9, no.4, pp.159-166, August 1974.

[16] C. Huang, Y. Peng, and C. Wang, "A BiCMOS Automatic Gain Control Amplifier for SONET OC-3," Proceedings of the Custom Integrated Circuits Conference, pp.103-106, 1995.

[17] M. Franciotta, G. Colli, and R. Castello, "A 100-MHz 4-mW Four-Quadrant BiCMOS Analog Multiplier," IEEE Journal of Solid-State Circuits, vol. 32, no.10, pp.1568-1572, Oct. 1997.

[18] Z. Wang, "A CMOS Four-Quadrant Analog Multiplier with Single-Ended Voltage Output and Improved Temperature Performance," IEEE Journal of Solid-State Circuits, vol. 26, no.9, pp.12931301, Sept. 1991.

[19] T. Ruotsalainen, P. Palojarvi, and J. Kostamovaara, "A Current Mode Gain-Control Scheme with Constant Bandwidth and Propagation Delay for a Transimpedance Preamplifier," IEEE Journal of Solid-State Circuits, vol. 34 no.2, pp.253-258, Feb. 1999.

[20] R. G. Meyer, and W. D. Mack, "A DC to 1-GHz Differential Monolithic Variable-Gain Amplifier," IEEE Journal of Solid-State Circuits, vol. 26, no.11, 1673-1680, Nov. 1991.

[21] E. A. M. Klumperink, C. T. Klein, B. Ruggeberg, and E. J. M. van Tuijl, "AM Suppression with Low AM-PM Conversion with the Aid of a Variable-Gain Amplifier," IEEE Journal of Solid_State Circuits., vol. 31, no.5, pp.625-633, May 1996.

[22] J. Hakkinen, T. Rahkonen, and J. Kostamovaara, "A 100-Mhz to 1 GHz Variable Gain Amplifier in a 8 GHz 1.2mm BiCMOS Process," Analog Integrated Circuits and Signal Processing, vol. 15, no.2, pp.169-181, Feb. 1998.

[23] K. E. Blake, "A Simplified-Transistor-Macromodel of a High-Speed Multiplier/ VGA," Midwest Symposium on Circuits and Systems, vol. 2, pp.1349-1352, 1993.

[24] D. A. Johns, and K. Martin, Analog Integrated Circuit Design, New York: Wiley, 1997.

[25] R. Gomez, and A. A. Abidi, "A 50 MHz Variable Gain Amplifier Cell in 2mm CMOS," IEEE 1991 Custom Integrated Circuits Conference, pp.9.4.1-3, 1991.

[26] R. Gomez, and A. A. Abidi, "A 50-MHz CMOS Variable Gain Amplifier for Magnetic Data Storage Systems," IEEE Journal of Solid-State Circuits, vol. 27, no.6, pp.935-939, June 1992.

[27] R. Harjani, "A Low-Power CMOS VGA for 50 Mb/s Disk Drive Read Channels," IEEE Transactions on Circuits and Systems II: Analog and Digital Proceesing, vol. 42, no.6, pp.370-376, June 1995.

[28] J. J. F. Rijns, "CMOS Low-Distortion High Frequency Variable-Gain Amplifier," IEEE Journal of Solid-State Circuits, vol. 31, no.7, pp.1029-1034, July 1996.

[29] K. Hadidi, and H. Kobayashi, "A 25 MHz 20 dB Variable Gain Amplifier," Conference Record IEEE Instrumentation and Measurement Technology Conference 2, pp.780-783, 1994.

[30] N. Kusayanagi, T. Choi, M. Hiwatashi, M. Segami, Y. Akasaka, and T. Wakabayashi, "A 25 Ms/s 8-b-10 Ms/s 10-b CMOS Data Acquisition IC for Digital Storage Oscilloscopes," IEEE Journal of Solid-State Circuits, vol. 33, no.3, pp.492-496, March 1998.

[31] P. J. G. van Lieshout, and R. J. van de Plassche, "A Monolithic Wideband Variable Gain Amplifier with a High Gain Range and Low Distortion," Digest of Technical Papers IEEE International Solid-State Circuits Conference, vol. 40, pp.358-359, Feb. 1997.

[32] P. J. G. van Lieshout, and R. J. van de Plassche, "A Power Efficient, Low-Distortion Variable Gain Amplifier Consisting of Coupled Differential Pairs," IEEE Journal of Solid-State Circuits, vol. 32, no.12, pp.2105-2110, Dec. 1997.

[33] L. H. Y. Leung, and A. Buchwald, "10-MHz 60-dB Dynamic-Range 6-dB Variable Gain Amplifier," Proceedings IEEE International Symposium on Analog Circuit and Signal Processing Neural Systems, pp.173-176, 1997.

[34] T. H. Hu, and P. R. Gray, "A Monolithic 480 Mb/s Parallel AGC/Decision/Clock-Recovery Circuit in 1.2-mm CMOS," IEEE Journal of Solid-State Circuits, vol. 28, no.12, pp.1314-1320, Dec. 1993.

[35] M. Muraguchi, and M. Aikawa, "A Linear Limiter: A 11-GHz Monolithic Low Distortion Variable Gain Amplifier," IEEE MTT S International Microwave Symposium Digest, vol. 2, pp.525-528, 1991.

[36] J. N. Babanezhad, and R. Gregorian, "A Programmable Gain/Loss Circuit," IEEE Journal of Solid-State Circuits, vol. SC-22, no.6, pp.1082-1090, Dec 1987.

[37] A.L. Wittenberg, M.L. Simpson, G.R. Young, R.L. Palmer, C.G. Moscone, and R.G. Jackson, "A CMOS Variable Gain Amplifier for PHENIX Electromagnetic Calorimeter and RICH Energy Measurements," IEEE Trans. Nuclear Sci., vol. 44, no.3, pp.326-330, June 1997.

[38] Analog Devices, Inc., High Speed Design Techniques, Norwood, MA: Analog Devices, Inc., 1996.

[39] J. Blaes, "A BiCMOS Digitally-Controlled Variable Gain Wideband Amplifier," Proceedings of the IEEE Bipolar BiCMOS Circuits and Technology Meeting, pp.84-87, 1997.

[40] E. Brunner, "An Ultra-Low Noise Linear-in-dB Variable Gain Amplifier for Medical Ultrasound Applications," Wescon Conference Record, pp.650-655, 1995.

[41] B. Gilbert, "A Low Noise Wideband Variable-Gain Amplifier Using an Interpolated Ladder Attenuator," IEEE ISSCC Technical Digest, pp.280, 281, 330, 1991.

[42] T. Ruotsalainen, P. Palojarvi, and J. Kostamovaara, "A BiCMOS Differential Anplifier and Timing Discriminator for the Reciever of a Lassar Radar," Analog Integrated Circuits and Signal Processing, vol. 13, no.3, pp.341-352, July 1997.

[43] P. W. Wallace, J. Bayruns, N. Scheinberg, M. Rachlin, and H. Krautter, "A Temperature Compensated L-Band Variable Gain Amplifier with Eight Bit Digital Control," Technical Digest GaAs IC Symposium 1oth Publ. by IEEE, pp.281-284, 1988.

[44] B. Razavi, Design of Analog CMOS Integrated Circuits, New York: McGraw-Hill, 2001.

[45] Avant! Corporation, HSPICE user manual, Avanti Corporation, Femont, CA, June 1999.

[46] S. D. Willingham, K. W. Martin, and A. Ganesan, "A BiCMOS Low-Distortion 8 MHz Low-Pass Filter," IEEE Journal of Solid-State Circuits, vol. 28, no.12, pp.1234-1245, Dec. 1993.

[47] W. Redman-White, "A High Bandwidth Constant gm and Slew-Rate Rail-to-Rail CMOS Input Circuit and its Application to Analog Cells for Low Voltage VLSI Systems," IEEE Journal of Solid-State Circuits, vol. 32, no.5, pp.701-712, May 1997.

[48] F. Yang, and C. C. Enz, "A Low-Distortion BiCMOS Seventh-Order Bessel Filter Operating at 2.5 V Supply," IEEE Journal of Solid-State Circuits, vol. 31, no.3, pp.321-330, March 1996.

[49] Z. Wang, and W. Guggenbuhl, "A Voltage-Controllable Linear MOS Transconductor Using Bias Offset Technique," IEEE Journal of Solid-State Circuits, vol. 25, no.1, pp.315-317, Feb. 1990.

[50] R. Alini, A. Baschirotto, and R. Castello, "Tunable BiCMOS Continuous-Time Filter for High-Frequency Applications," IEEE Journal of Solid-State Circuits, vol. 27, no.12, pp.1906-1915, Dec. 1992.

[51] H. Tanimoto, M. Koyama, and Y. Yoshida, "Realization of a 1-V Active Filter Using a Linearization Technique Employing Plurality of Emitter-Coupled Pairs," IEEE Journal of Solid-State Circuits, vol. 26, no.7, pp.937-945, July 1991.

[52] C. H. J. Mensink, B. Nauta, and H. Wallinga, "A CMOS 'Soft-Switched' Transconductor and Its Application in Gain Control and Filters," IEEE Journal of Solid-State Circuits, vol. 32, no.7, pp.989-998, July 1997.

[53] J. Silva-Martinez, M. S. J. Steyaert, and W. M. C. Sansen, "A Large-Signal Very Low-Distortion Transconductor for High-Frequency Continuous-Time Filters," IEEE Journal of Solid-State Circuits, vol. 26, no.7, pp.946-955, July 1991.

[54] D.M. Binkley, Internal Document, Concorde Microsystems, Inc., Knoxville, Tennessee, 2000.

[55] Maxim Integrated Products, MAX 436 data sheet, Maxim, Inc., 2001.

Vita

Bryan Scott Puckett was born in Lubbock, Texas on July 25, 1968. Most of his childhood was spent in Portland, Tennessee, where he graduated from Highland Academy in 1987. Bryan continued his education at Southern College of Seventh-day Adventists in Collegedale, TN. He graduated in 1991 with a B.S. in mathematics and a second major in physics. He attended Vanderbilt Unversity for two years studying graduate physics. After Vanderbilt, he attended the University of Tennessee at Knoxville where he recieved his B.S.E.E. in December of 1995, his M.S. in Electrical Engineering in August of 1998, and his Ph.D. in Electrical Engineering in December of 2001.